

Triathlon

Schematics Document

Mobile Yonah uFCPGA with Intel
Calistoga_GM/PM+ICH7-M core logic

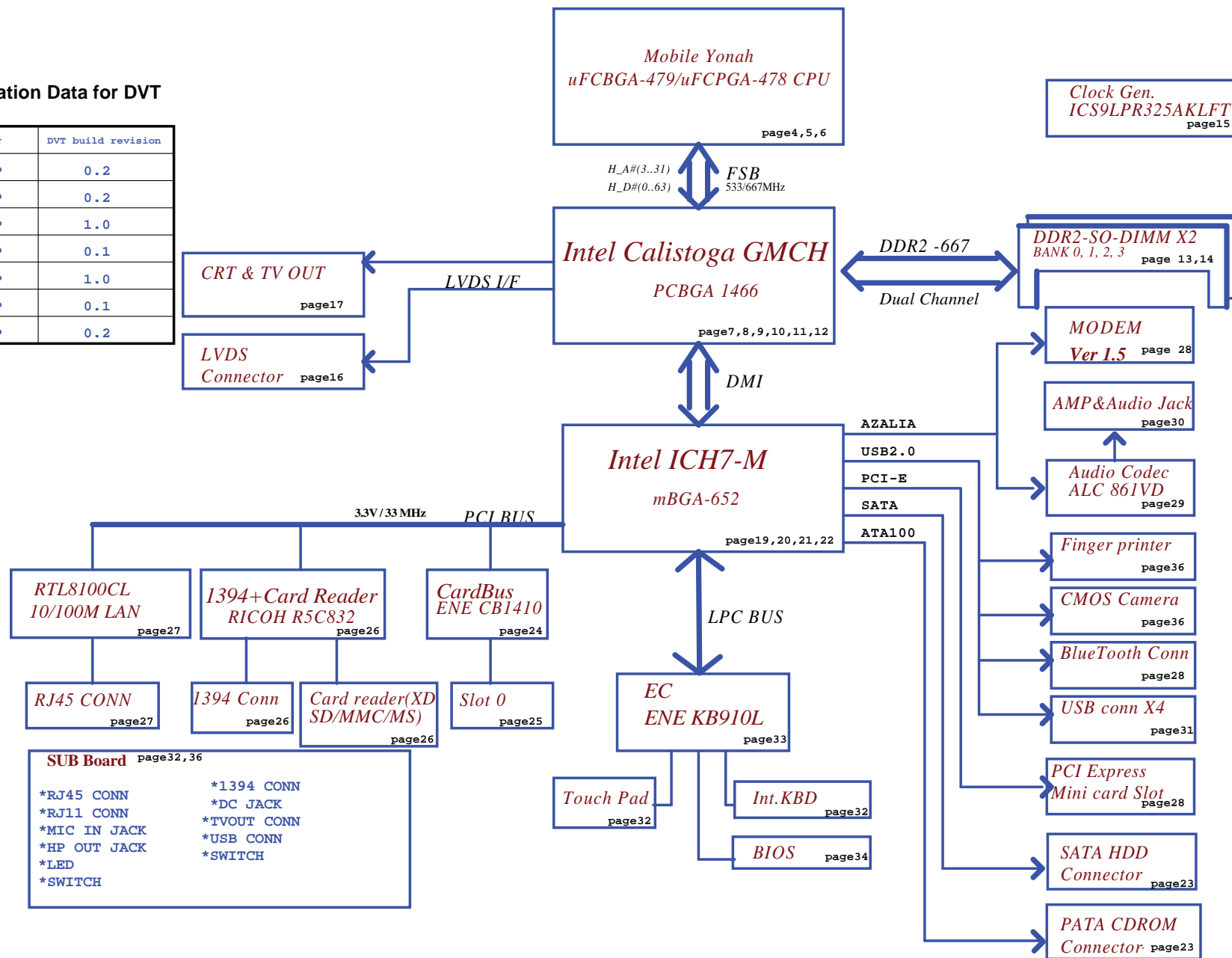
星期三, 七月 12, 2006

REV:0.3

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HDL20 PCB panelization Data for DVT

PCB Function	PCB Number	DVT build revision
MB	LA3281P	0.2
Audio/USB	LS3251P	0.2
SW board	LS3102P	1.0
CRT board	LS3253P	0.1
TP board	LS3104P	1.0
FP Board	LS3255P	0.1
LED board	LS3256P	0.2



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Voltage Rails

power plane State				+5VS +3VS +2.5VS +1.8VS +1.5VS +1.2VS +VGA_CORE +0.9VS +CPU_CORE +VCCP
	+B LDO3 LDO5	+5VALW +3VALW	+1.8V +5V	
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON
X MEANS OFF

S3 : STR
S4 : STD
S5 : SOFT OFF

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
1394	AD22	0	PIRQG/H
LAN	AD17	3	PIRQF
CardBus	AD20	2	PIRQA

EC SM Bus1 address

Device	Address	Device	Address
Smart Battery	0001 011X b	ADM1032	1001 100X b
EEPROM(24C16/02)	1010 000X b		

EC SM Bus2 address

ICH6 SM Bus address

Device	Address
Clock Generator (ICS954226)	1101 001Xb
DDRII DIMM0	1010 000Xb
DDRII DIMM1	1010 010Xb

SKU ID Table

Vcc	3.3V +/- 5%			
Ra	100K +/- 5%			
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max
* 0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

SKU ID	MB ID(H)	MB ID(L)
0		
1		
2		
3	HDL10	HDL00
* 4		HDL20
5	IDL12	HDL30
6		
7		

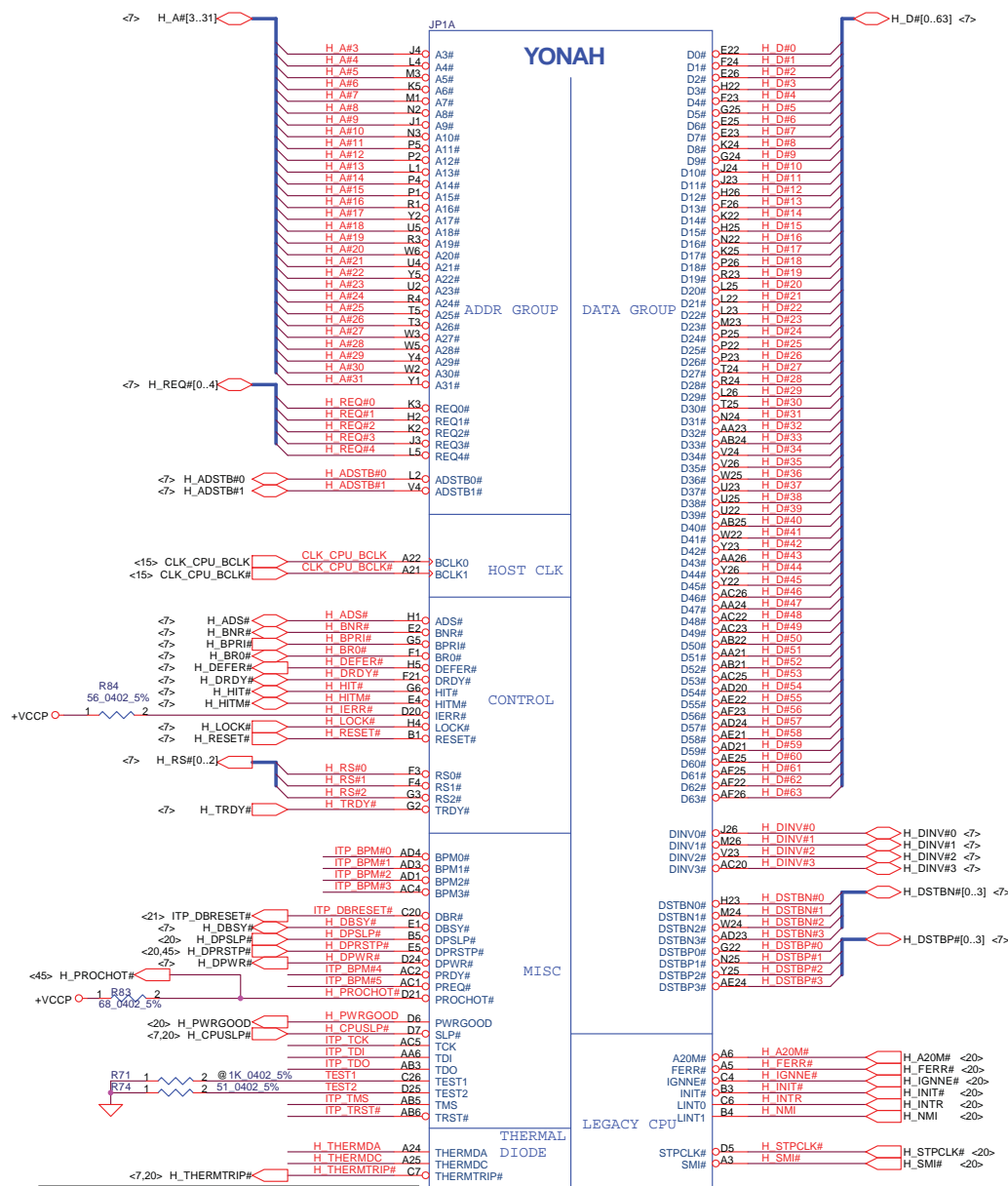
	MB ID
H	15"
L	14"

BOM Structure

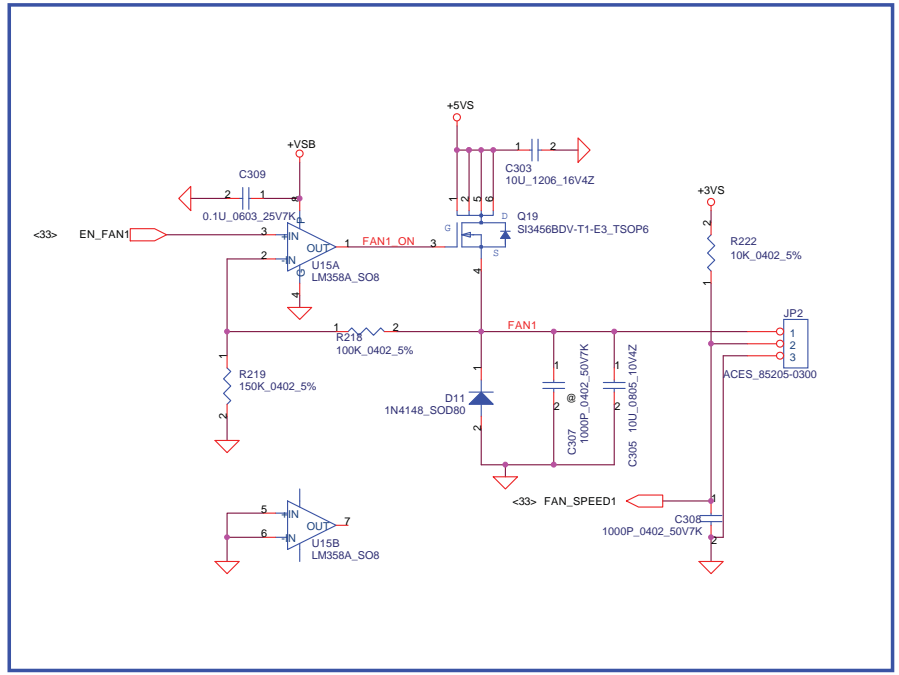
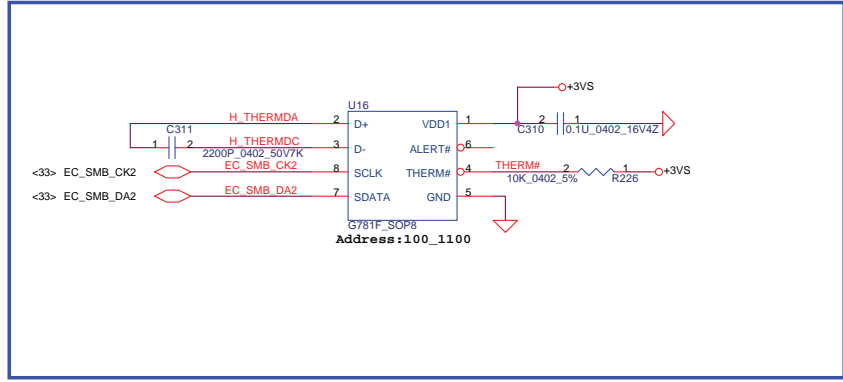
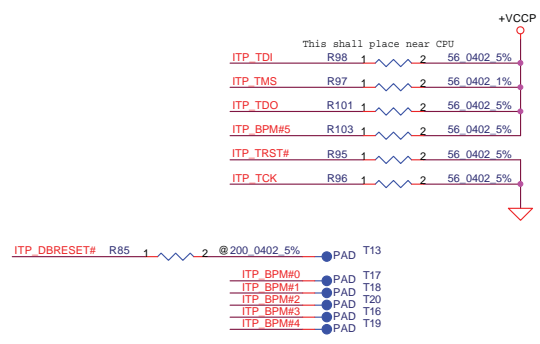
MARK	FUNCTION
@	NC FOR ALL
GIGA@	8110SBL(SCL)Giga LAN
10/100@	8100CL 10/100Mb LAN
UMA@	Internal 945GM
VGA@	External G7xM

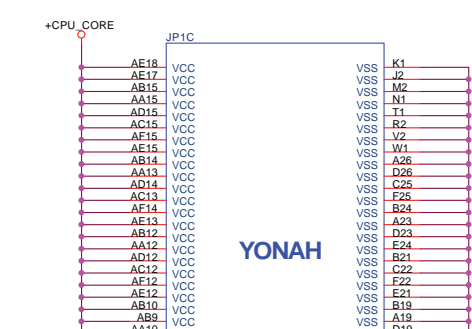
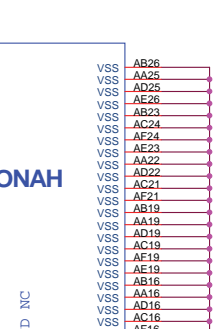
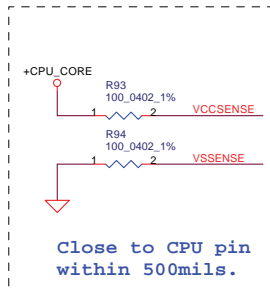
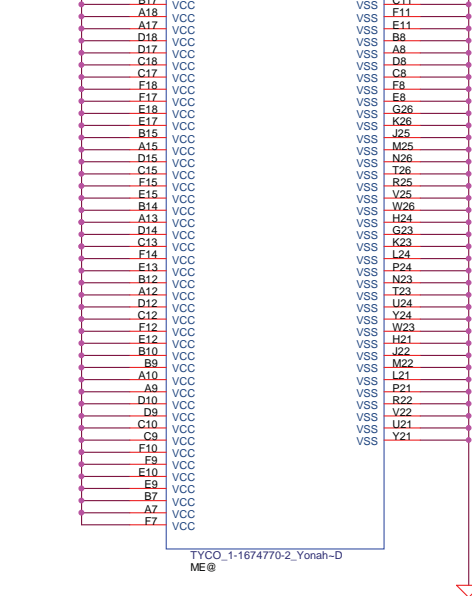
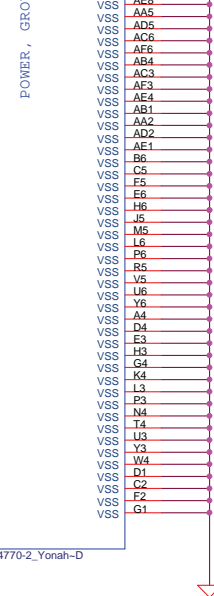
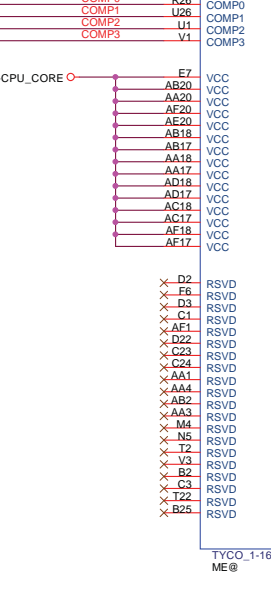
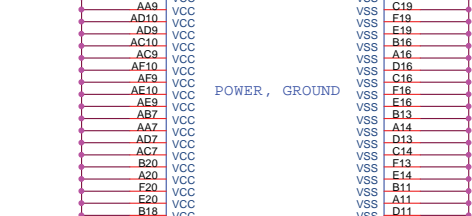
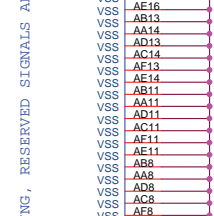
USB PORT LIST

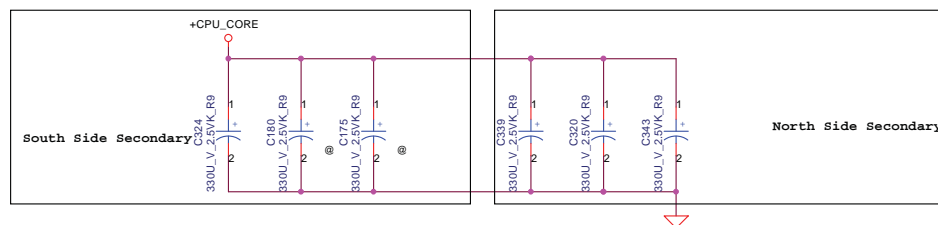
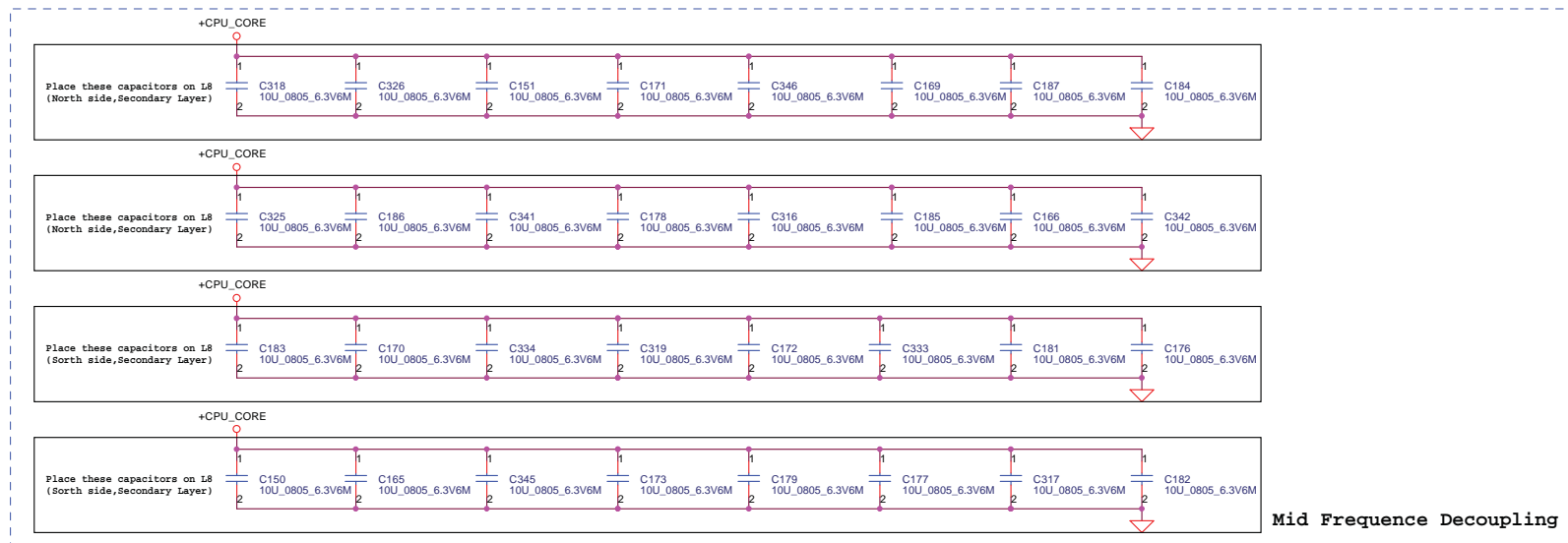
PORT	DEVICE
0	LEFT SIDE
1	BT(HDL00/10)
2	RIGHT SIDE
3	CMOS
4	RIGHT SIDE
5	FINGER PRINTER
6	RIGHT SIDE
7	BT(HDL20)



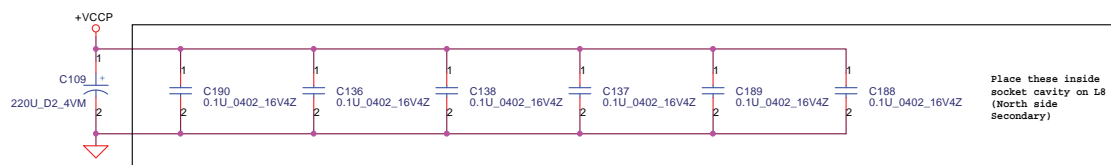
H_THERMDA, H_THERMDC routing together.
Trace width / Spacing = 10 / 10 mil



[illegible]

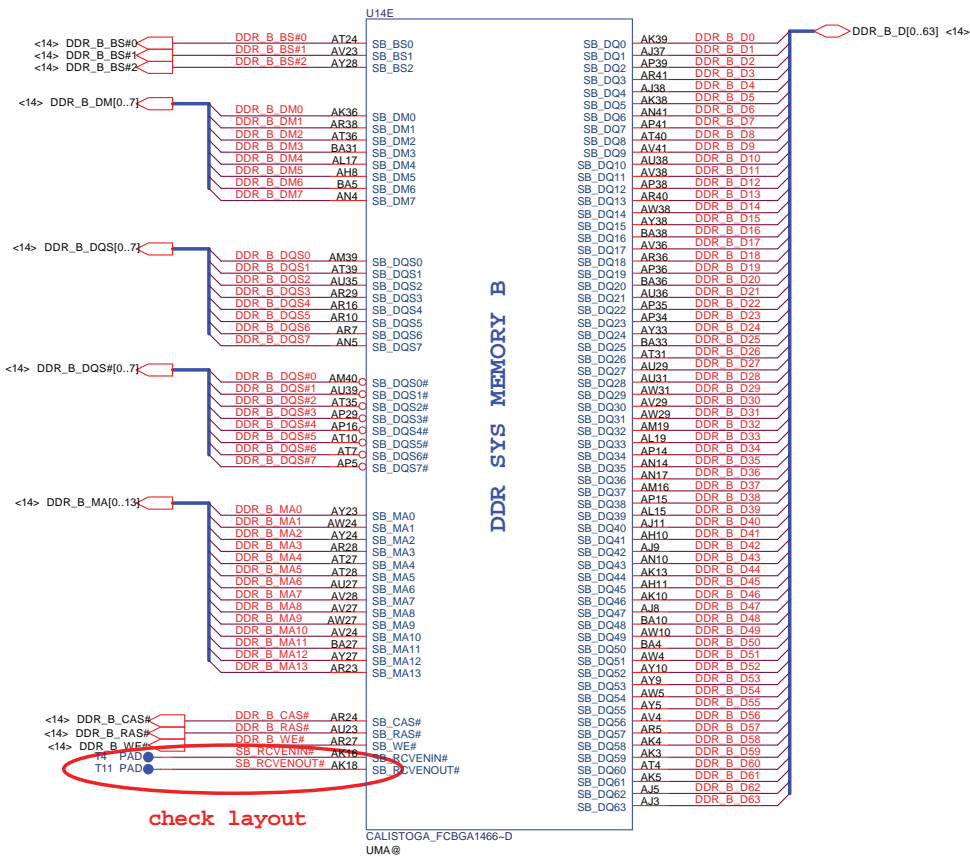
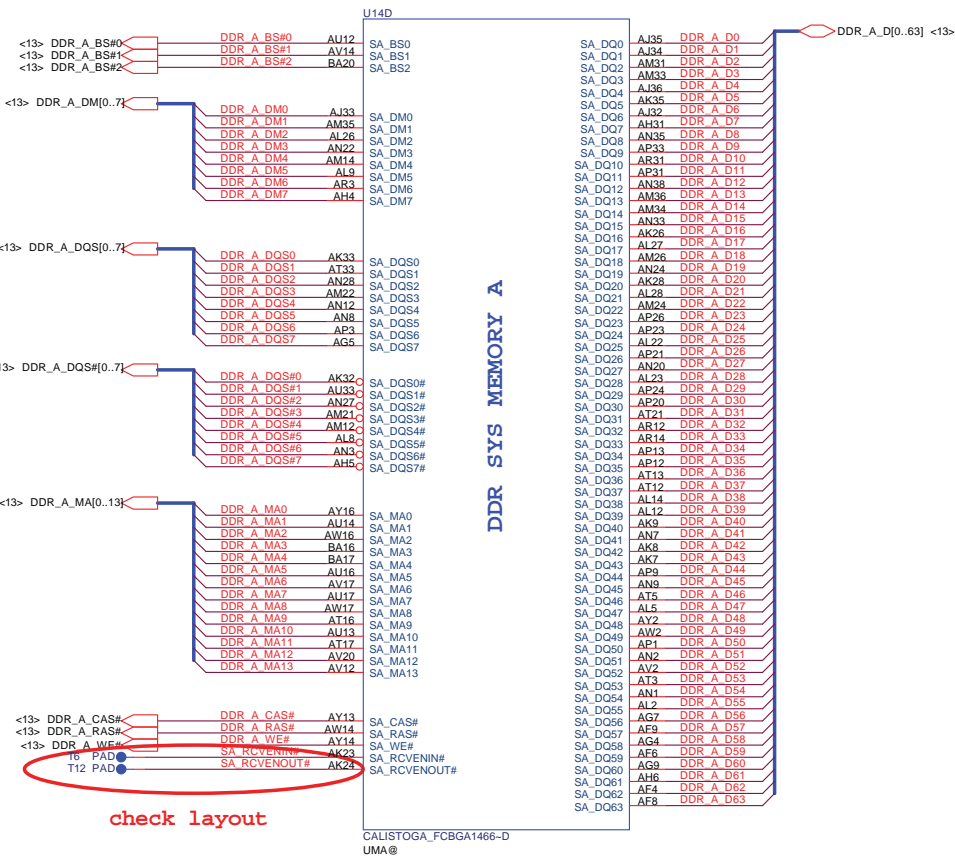


ESR <= 1.5m ohm
Capacitor > 1980uF

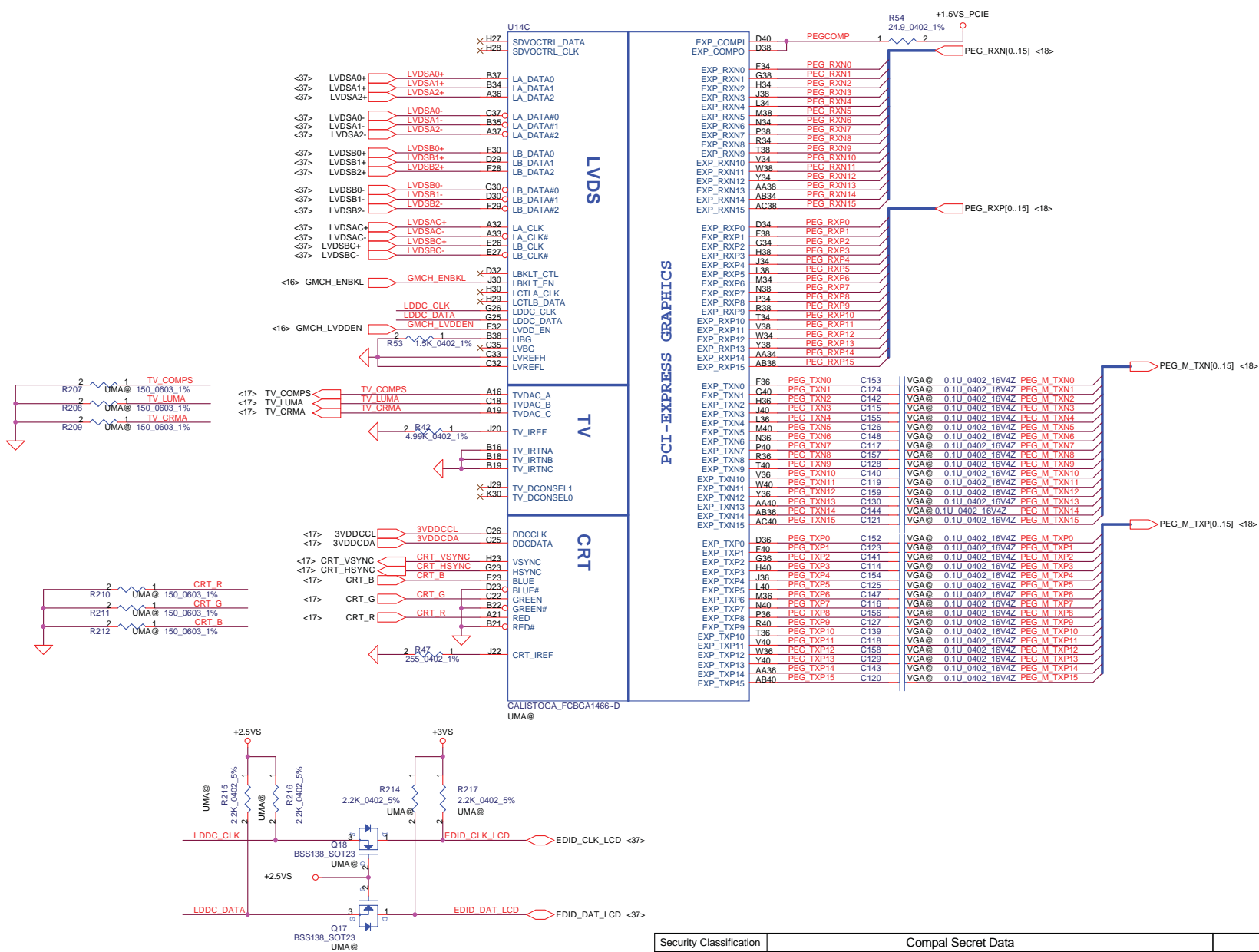


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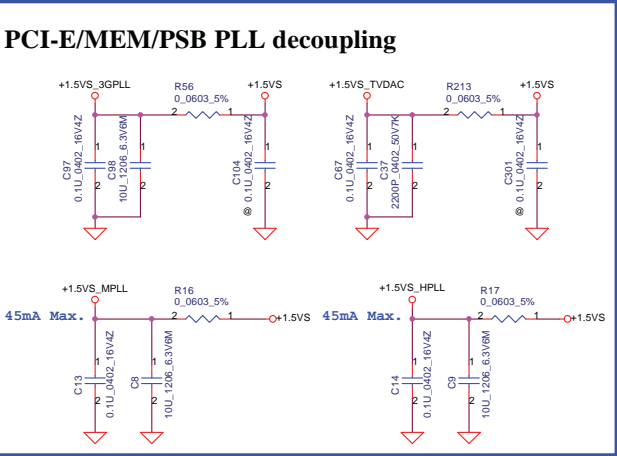
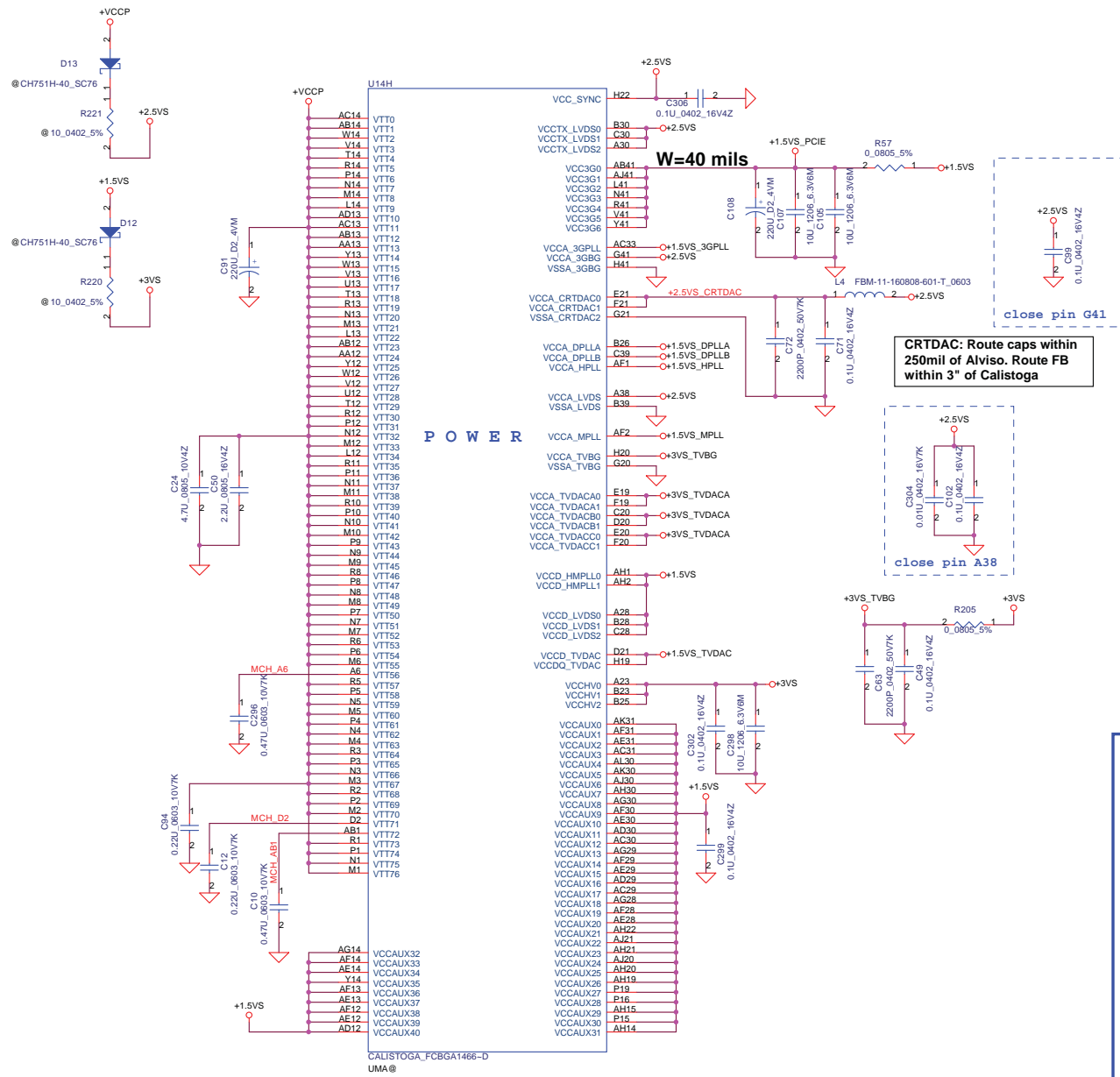




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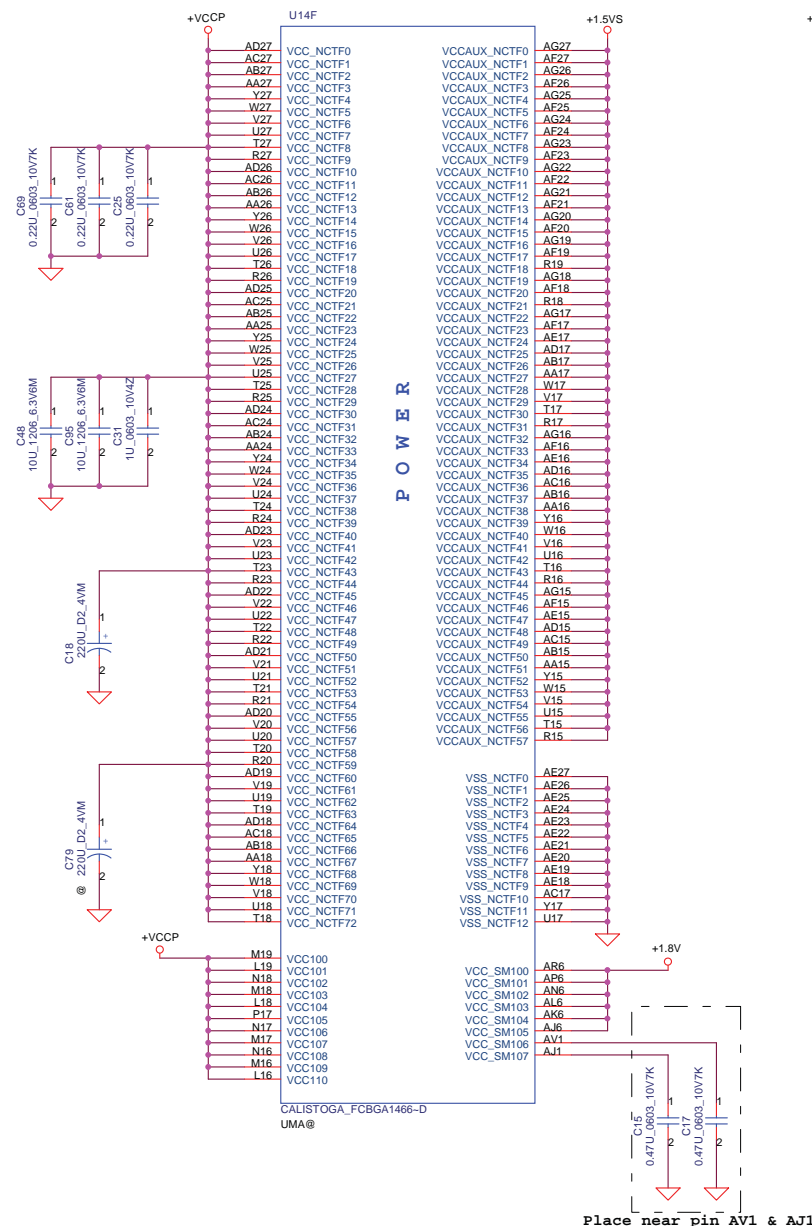
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Strap Pin Table

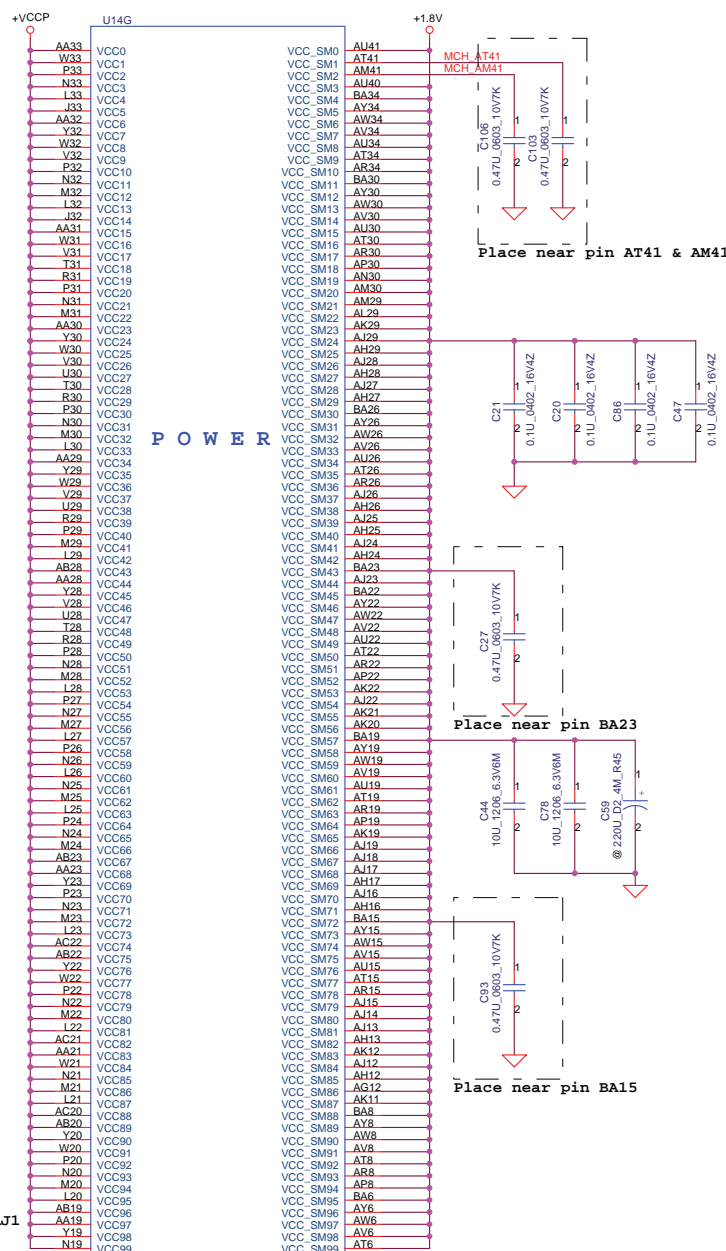
CFG[3:17] have internal pull up
CFG[19:18] have internal pull down

CFG[2:0]	011 = 667MT/s FSB 001 = 533MT/s FSB
CFG5	0 = DMI x 2 1 = DMI x 4 *(Default)
CFG7	0 = Reserved 1 = Mobile Yonah CPU*(Default)
CFG9	0 = Lane Reversal Enable 1 = Normal Operation (Default)*
CFG6	0 = Reserved 1 = Calistoga *
PSB 4X CLK Enable	
CFG[13:12]	00 = Reserved 01 = XOR Mode Enabled 10 = All Z Mode Enabled 11 = Normal Operation *(Default)
CFG16	0 = Dynamic ODT Disabled 1 = Dynamic ODT Enabled *(Default)
CFG10 CFG18	10 = 1.05V*(Default) 01 = 1.5V
CFG19	0 = Normal Operation *(Default) 1 = DMI Lane Reversal Enable
SDVO_CTRLDATA	0 = No SDVO Device Present *(Default) 1 = SDVO Device Present
CFG20 (PCIE/SDVO select)	0 = Only PCIE or SDVO is operational. *(Default) 1 = PCIE/SDVO are operating simu.



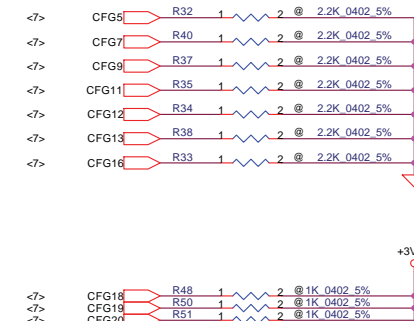
CALISTOGA_FCBGA1466-D
UMA@

Place near pin AV1 & AJ1



CALISTOGA_FCBGA1466-D
UMA@

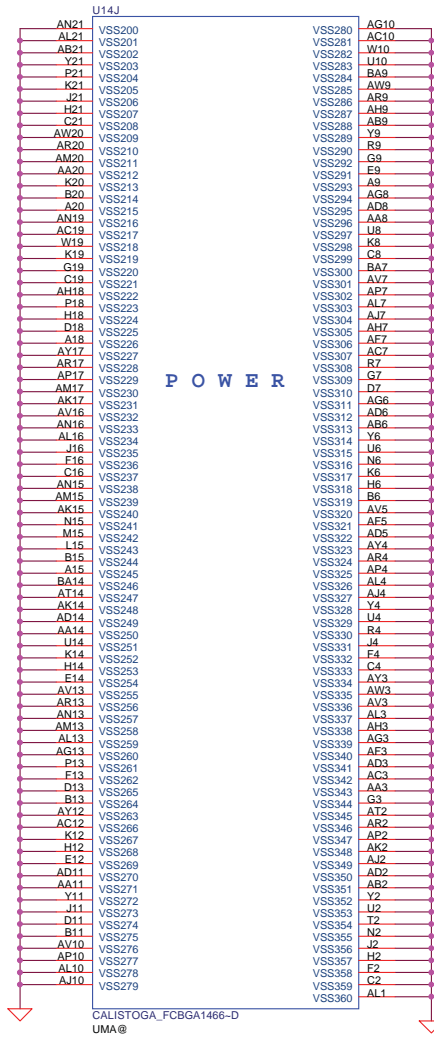
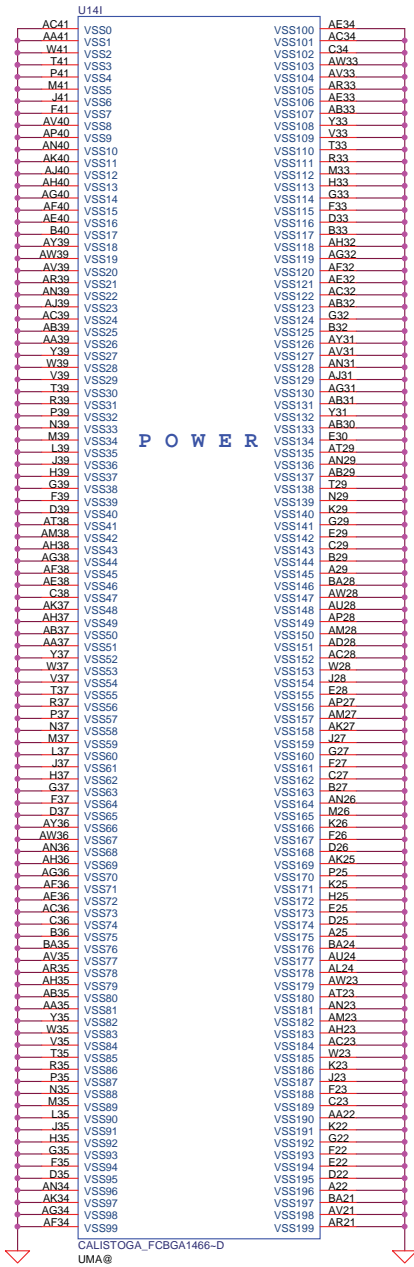
Place near pin BA15



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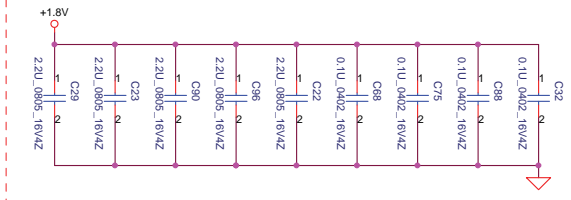
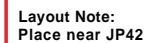
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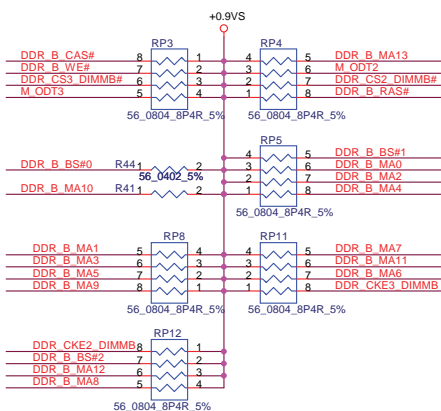
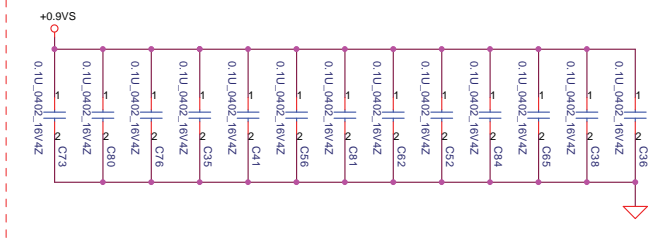


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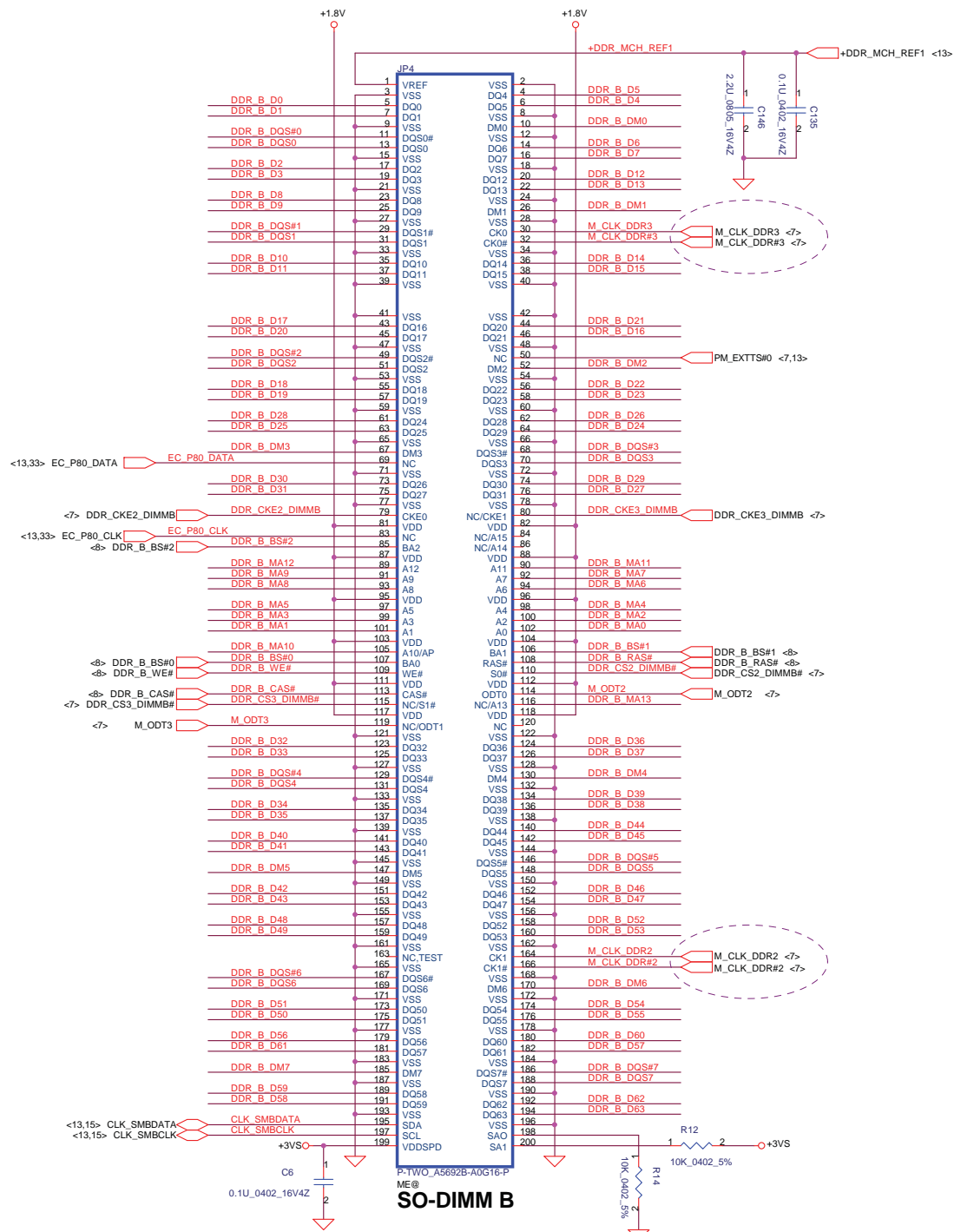




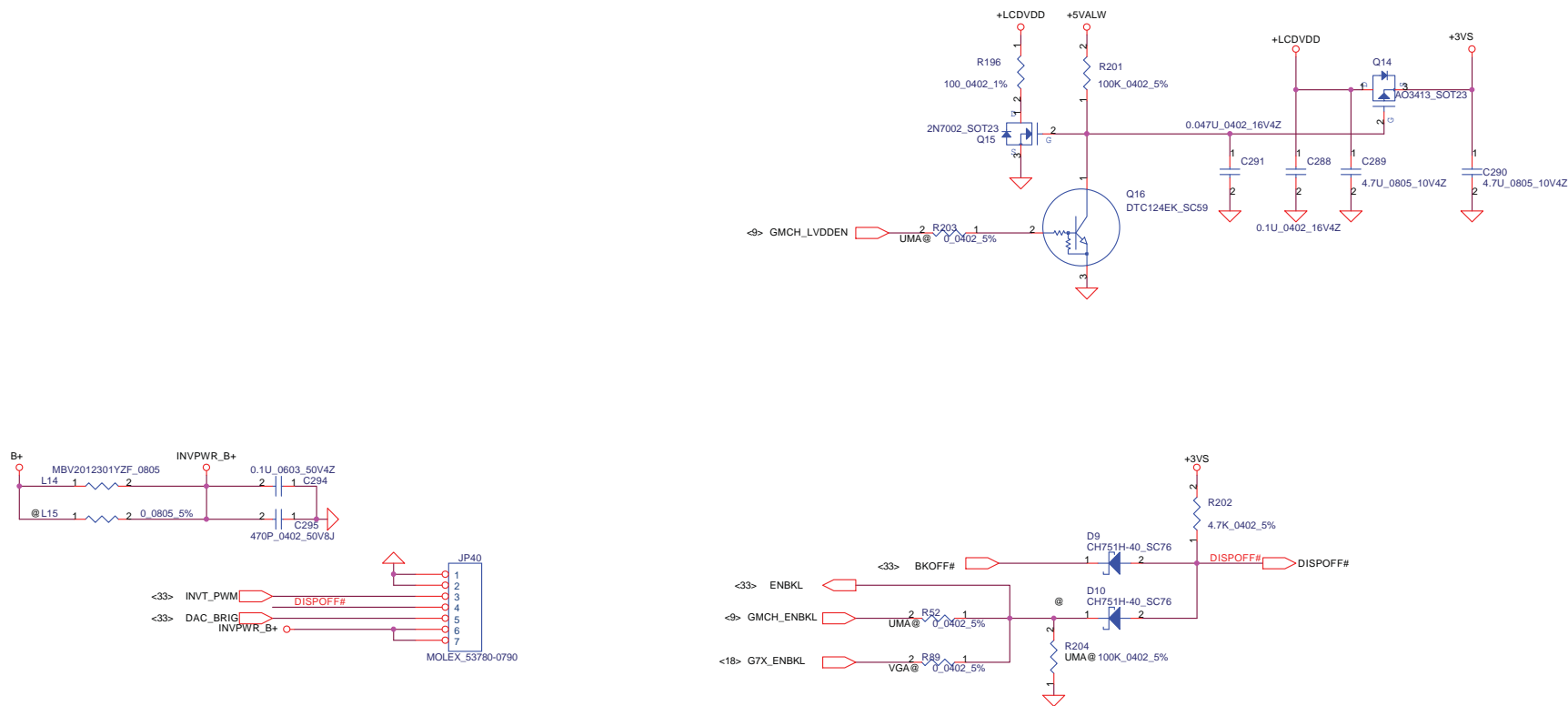
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9VS



Layout Note:
Place these resistor
closely JP42,all
trace length Max=1.5"

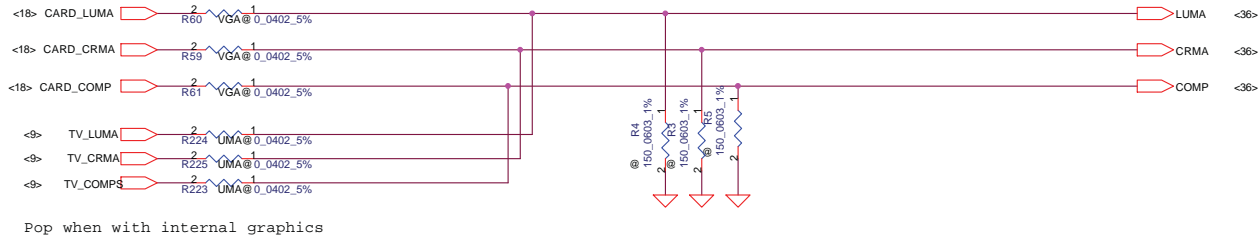


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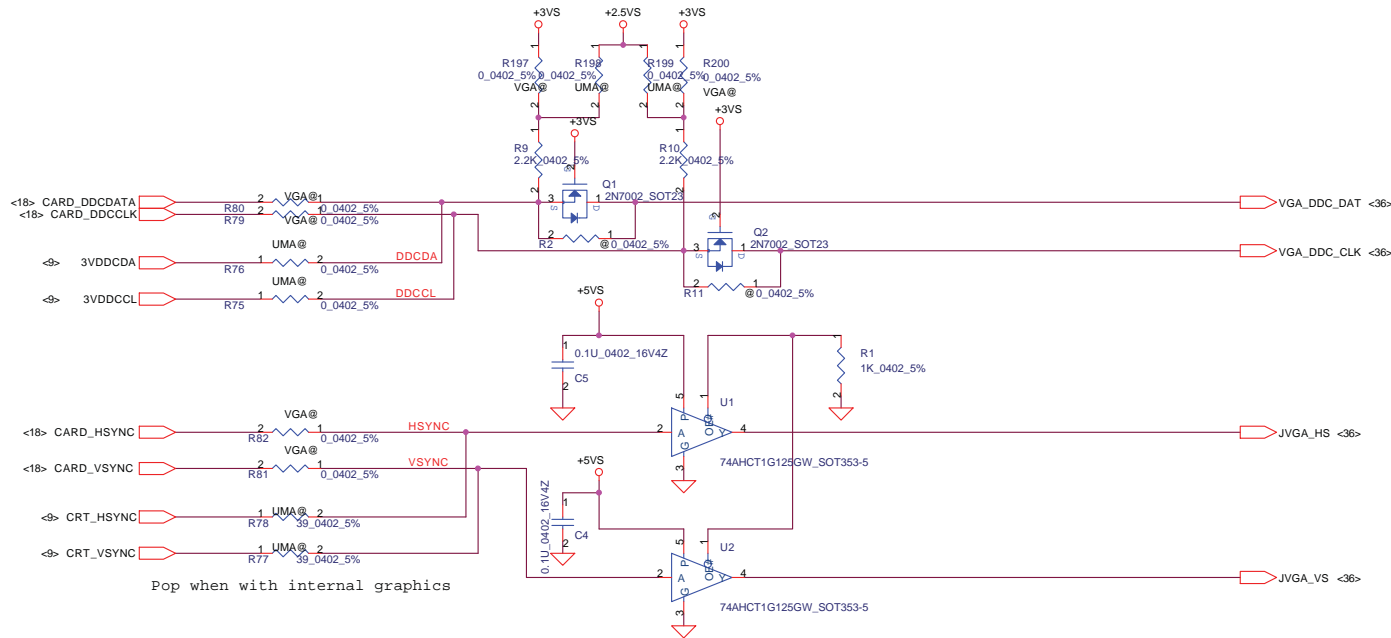
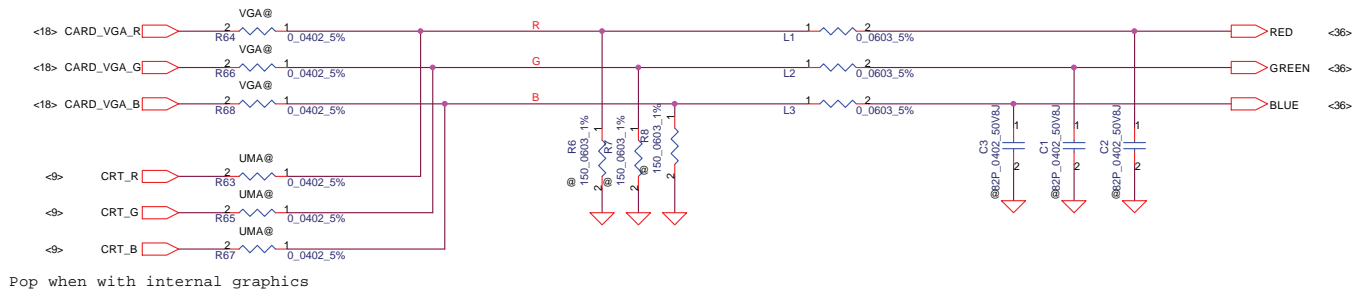


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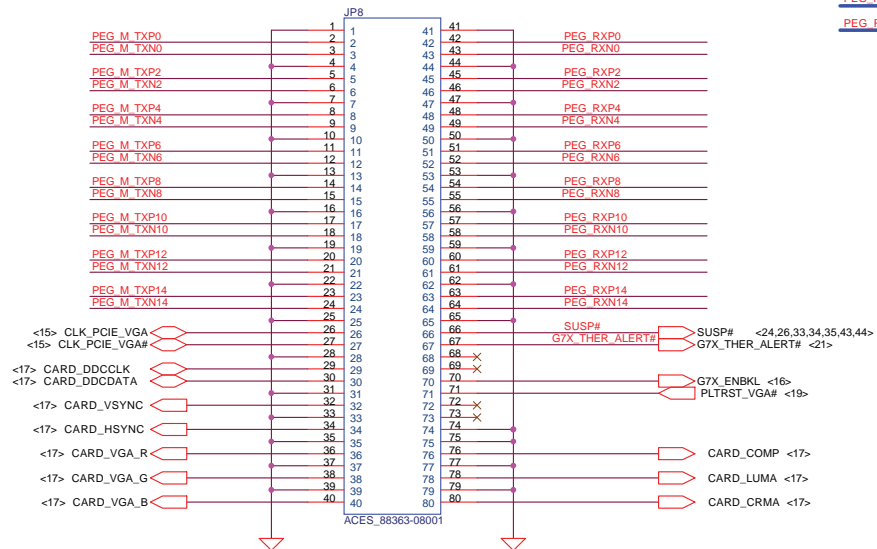
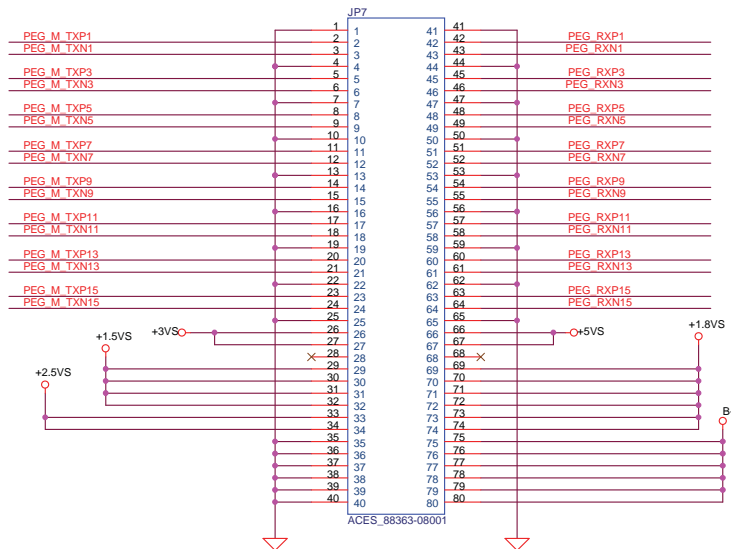
TV-OUT Conn.



CRT Conn.

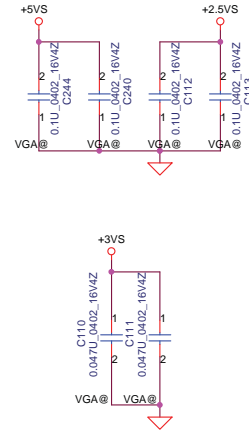


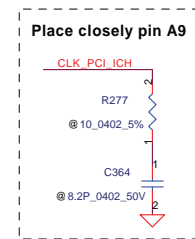
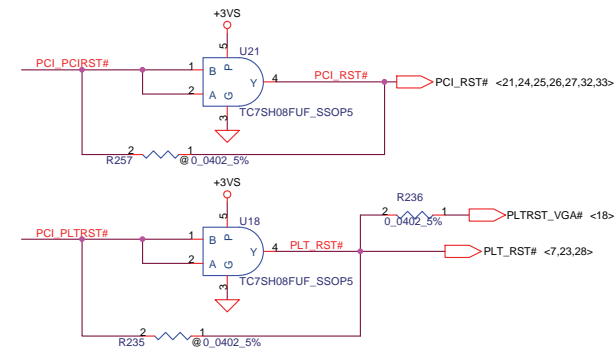
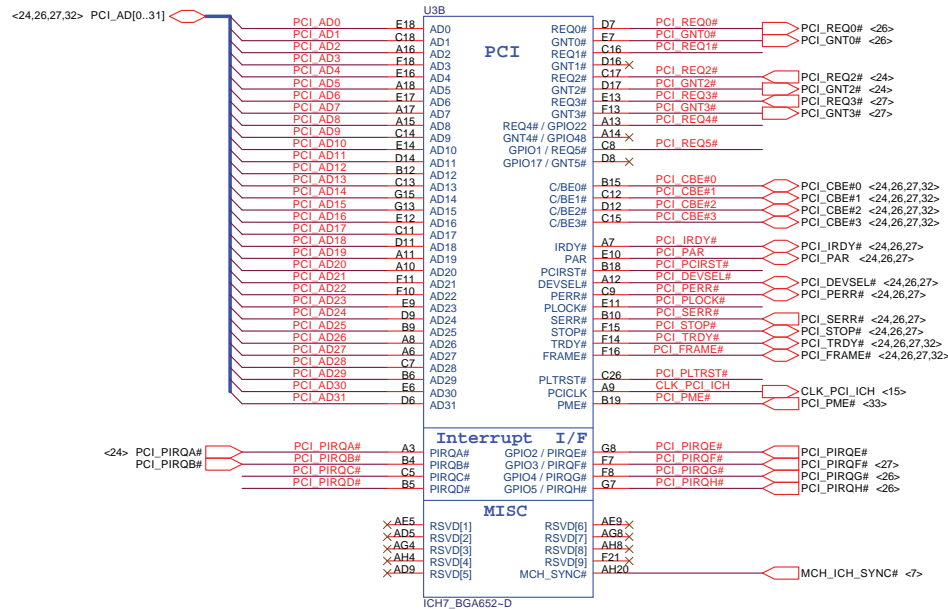
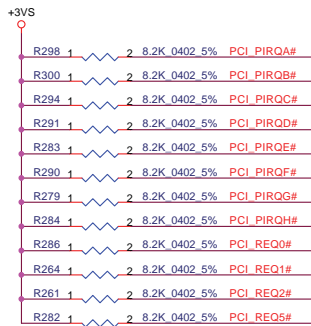
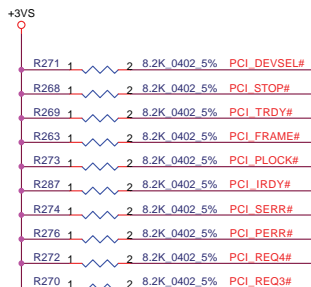
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MAX. 4.06A @ 1.8V
MAX. 130mA @ 2.5V
MAX. 655mA @ 3.3V

PEG M_TXP[0..15] PEG_M_TXP[0..15] <9>
PEG M_TXN[0..15] PEG_M_TXN[0..15] <9>
PEG_RXP[0..15] PEG_RXP[0..15] <9>
PEG_RXN[0..15] PEG_RXN[0..15] <9>

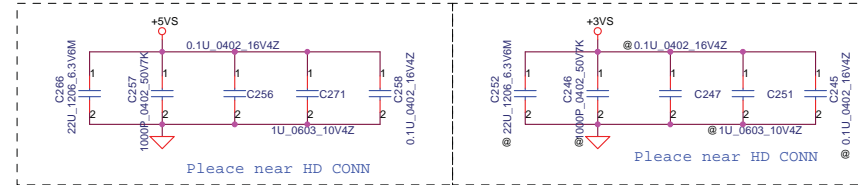
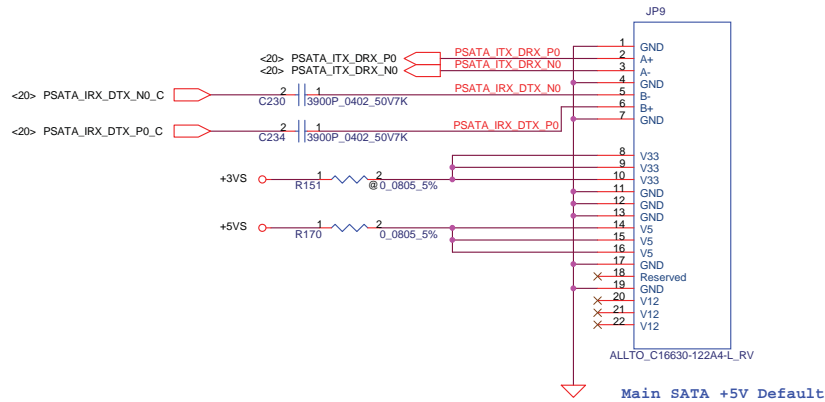




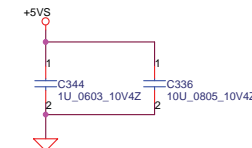
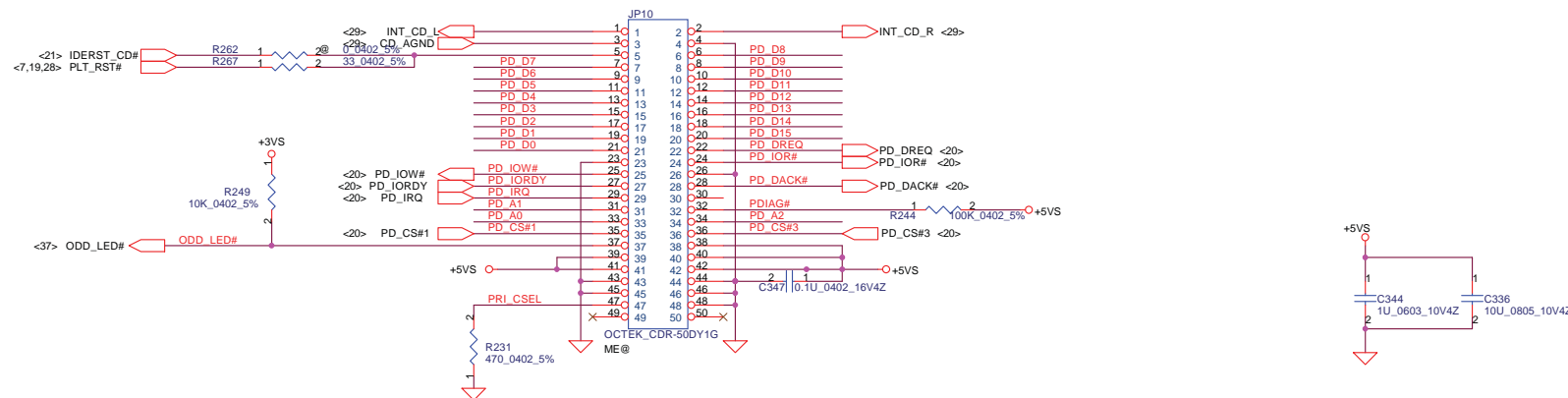
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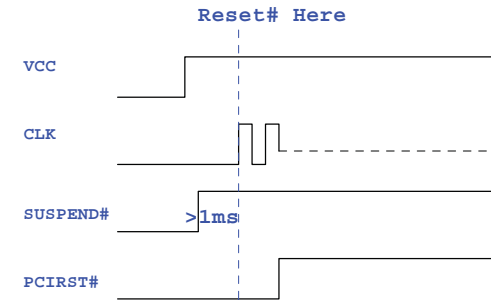


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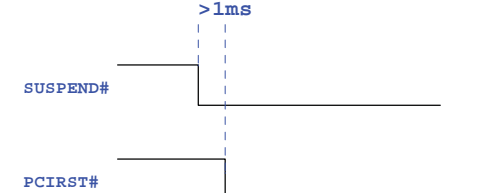


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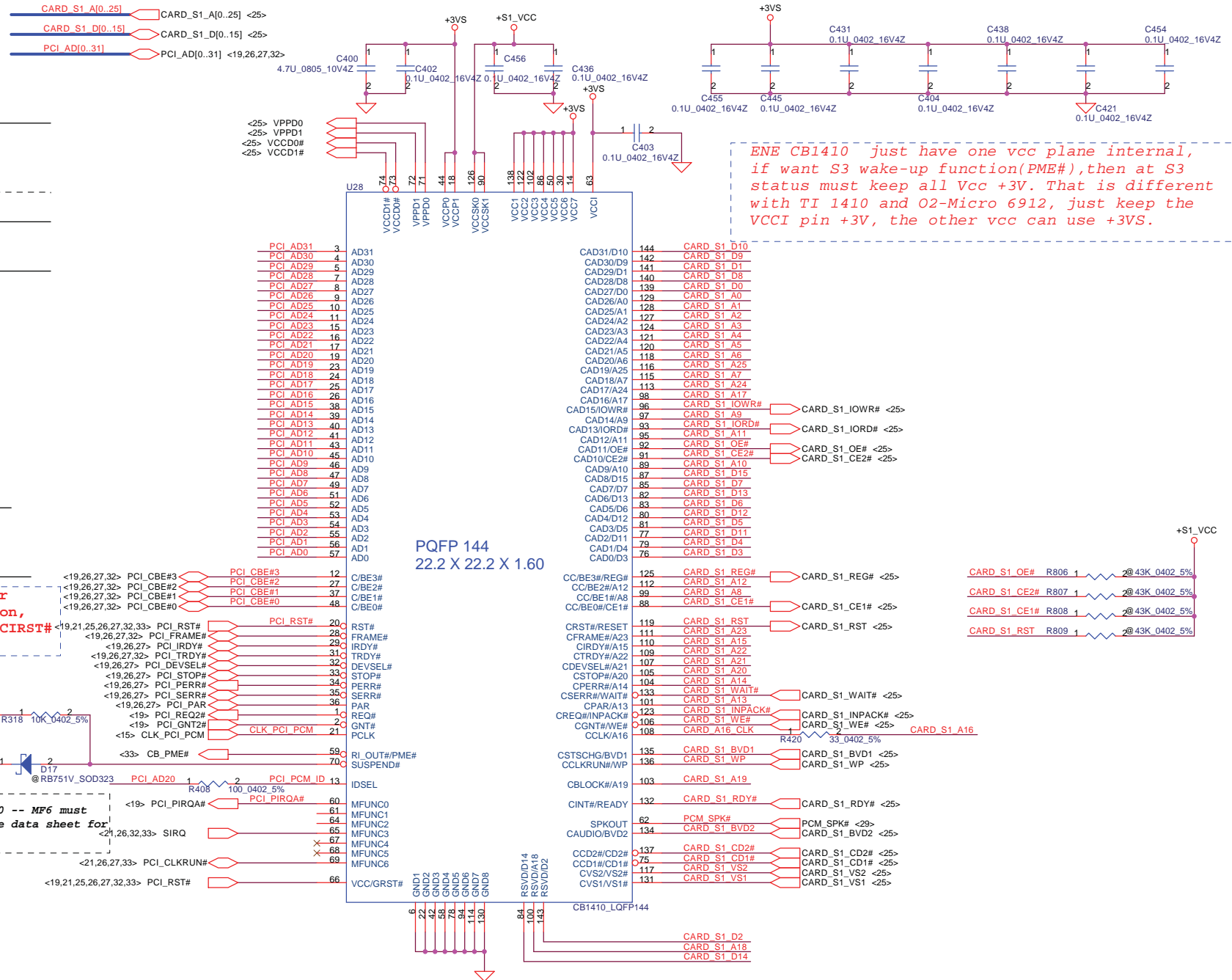
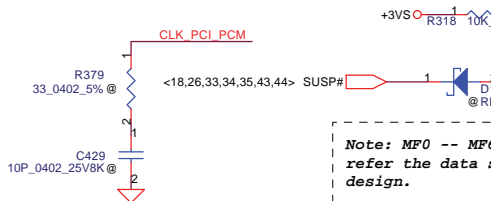
Power on RESET#



Entry S3

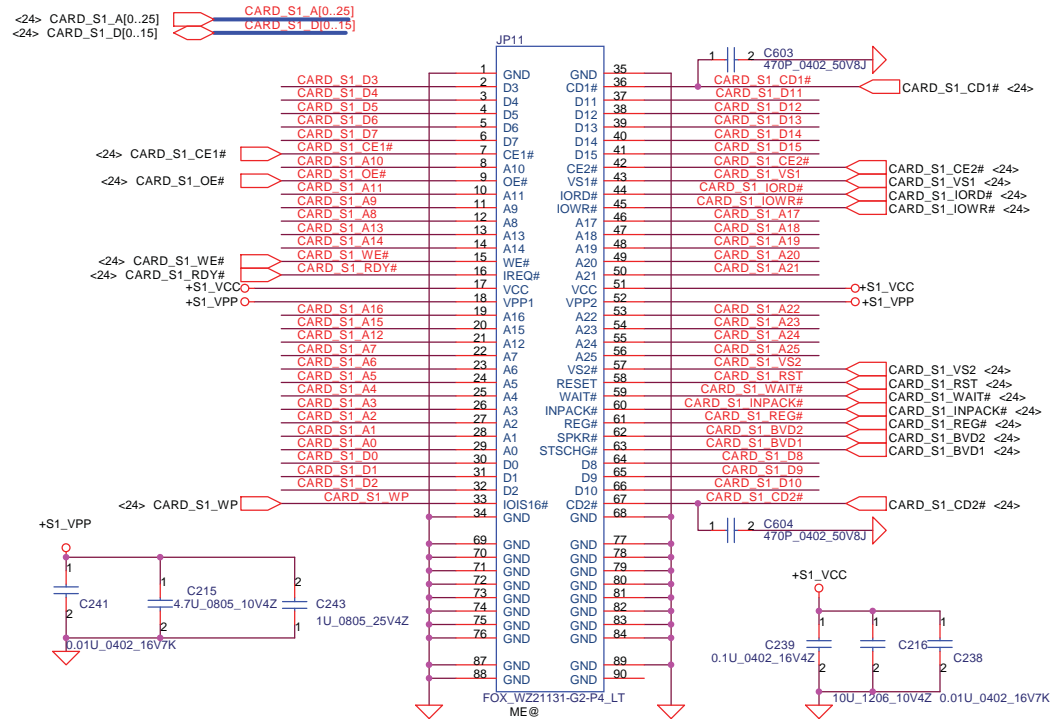


SUSPEND# will gate the PCIRST# or GRST#, so need S3 wake up function, SUSPEND# must be LOW ahead the PCIRST# about 1ms.

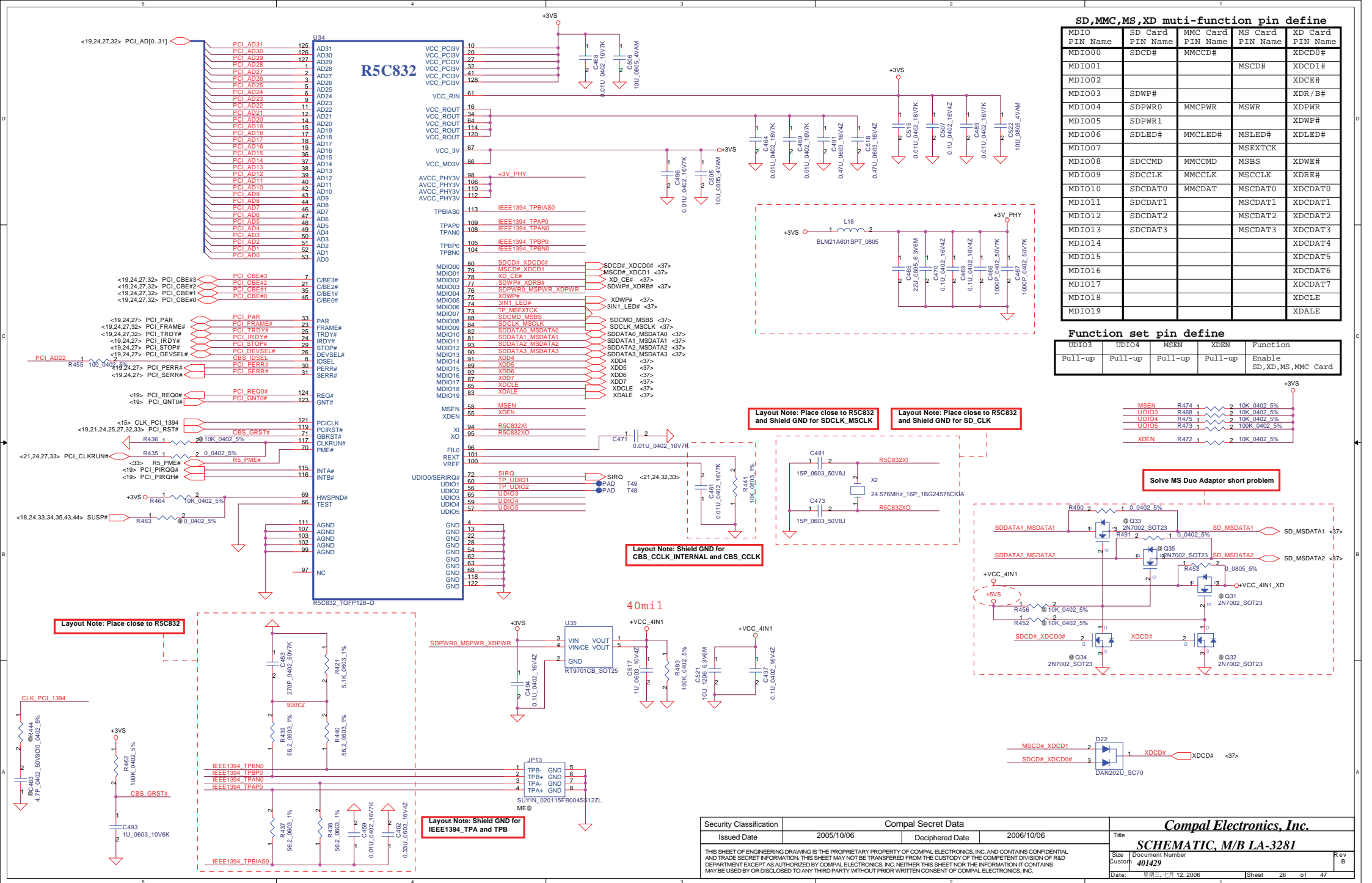


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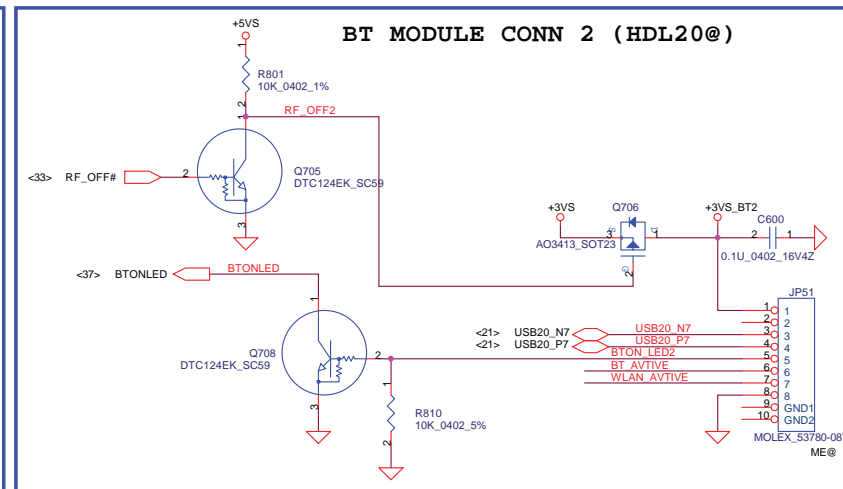
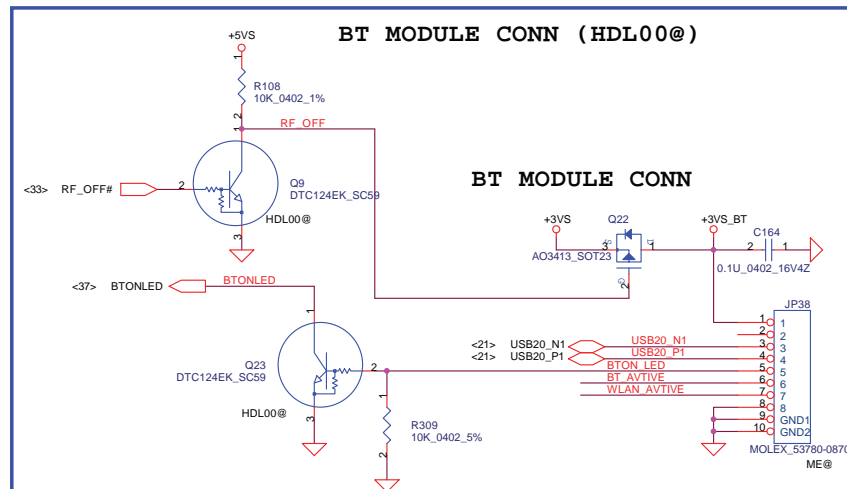
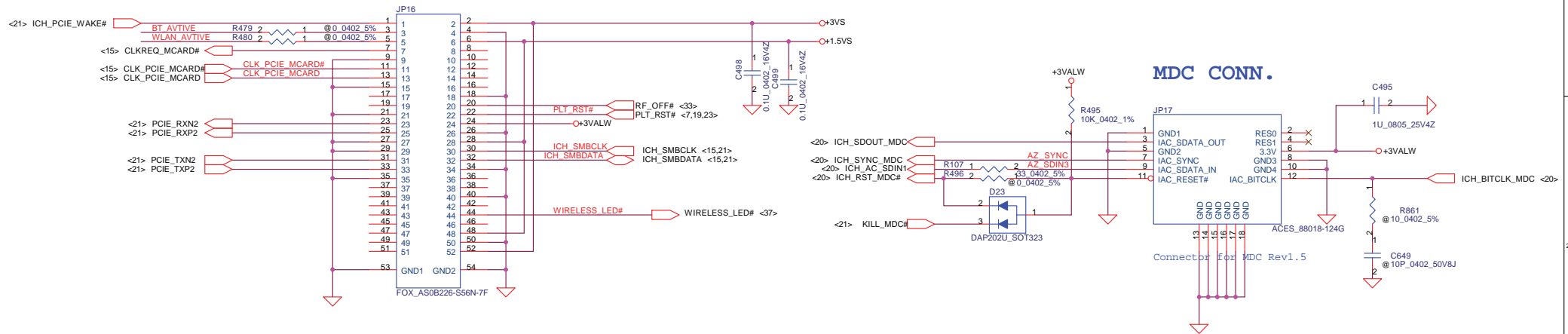
WWW.AliSaler.Com



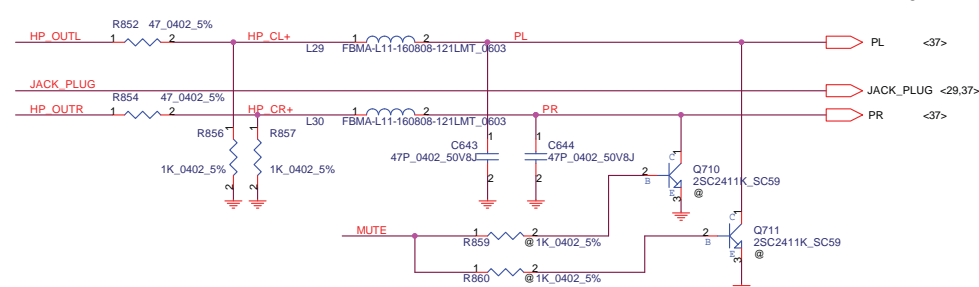
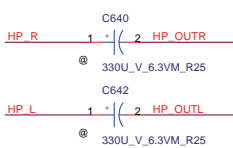
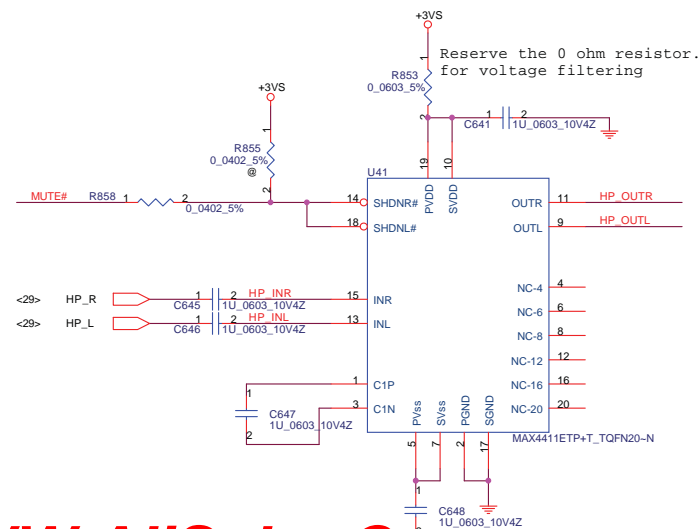
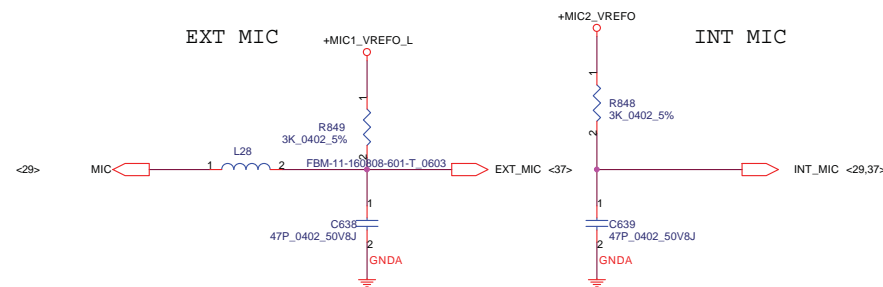
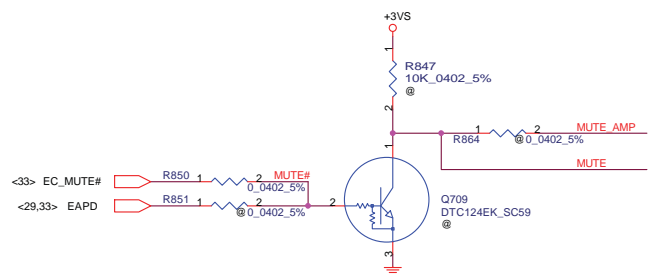
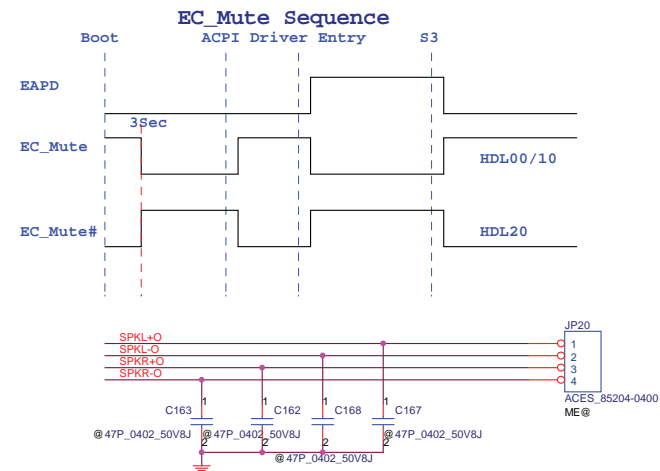
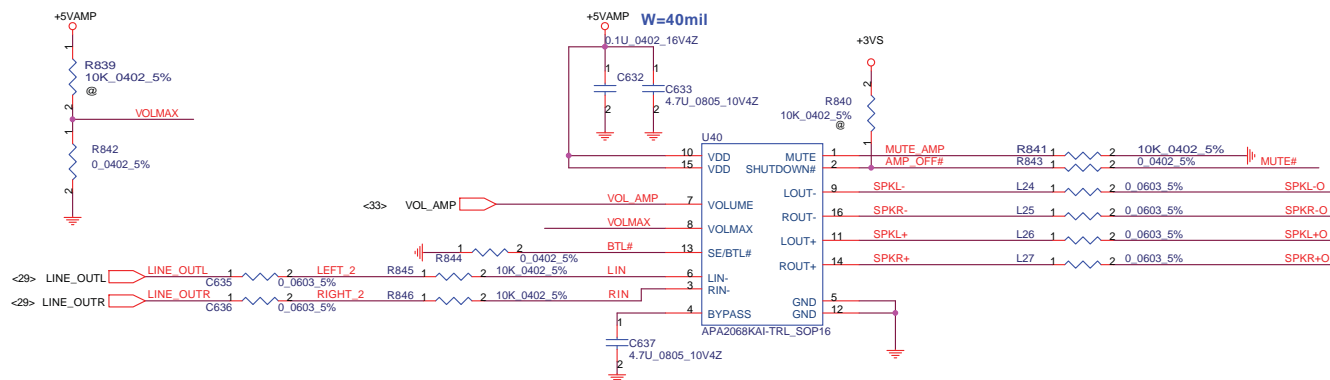
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Mini-Express Card(Slot 1-WLAN)



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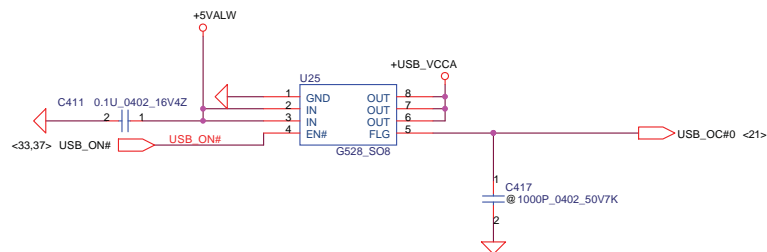
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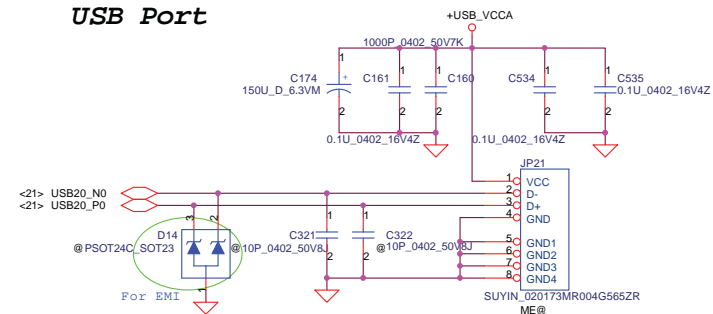
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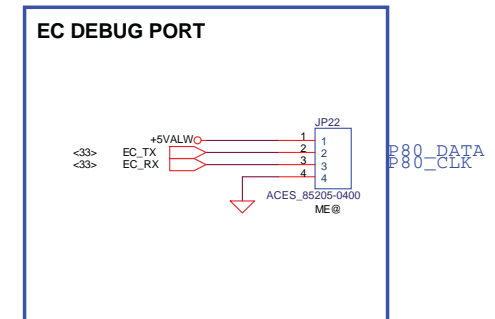
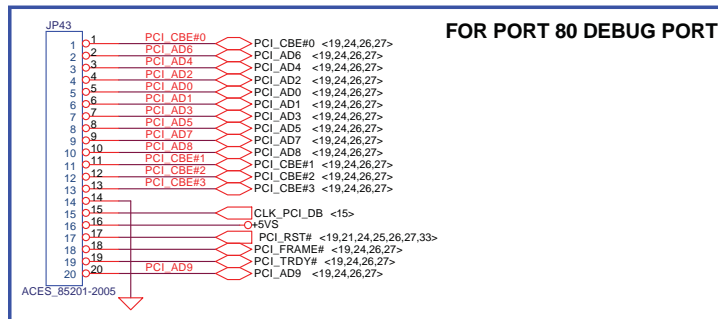
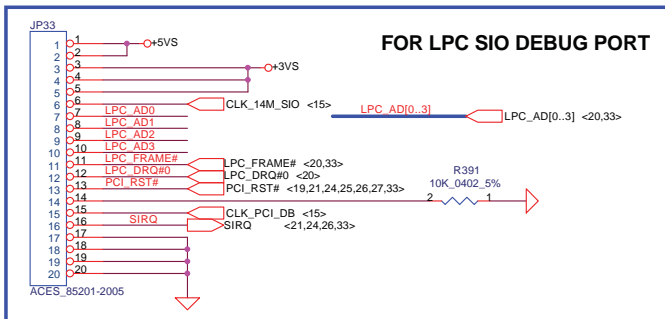
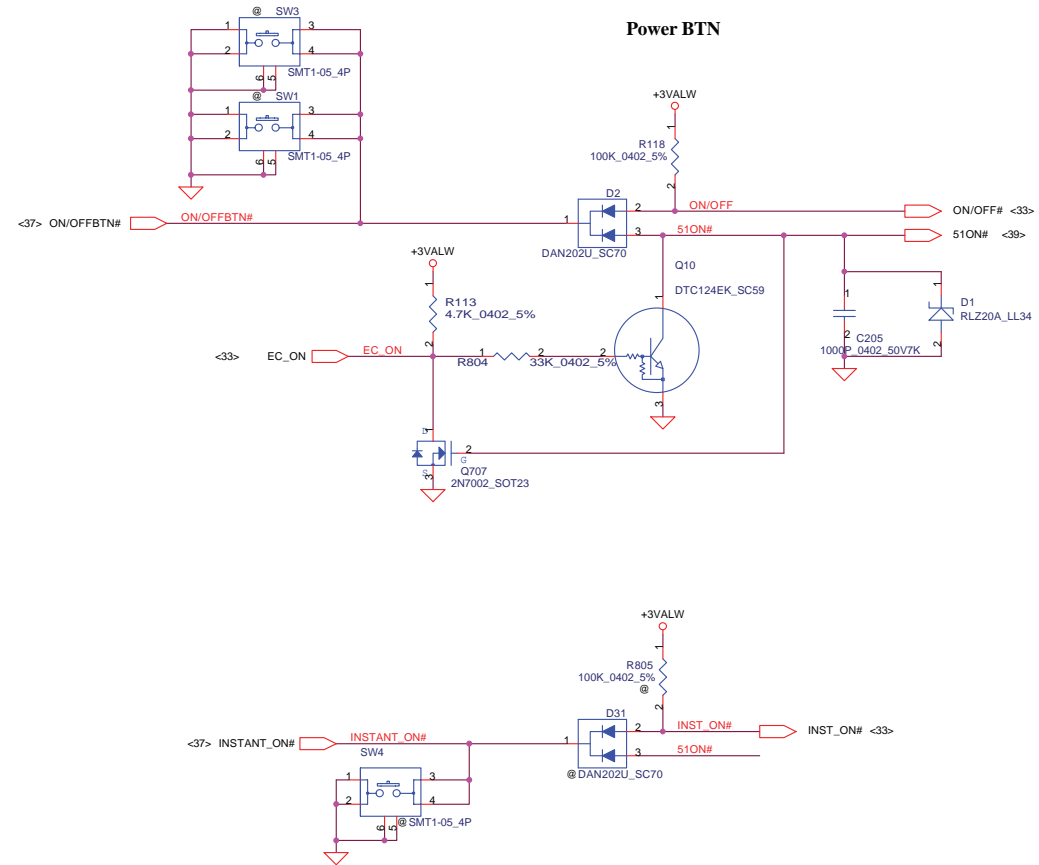


USB Port



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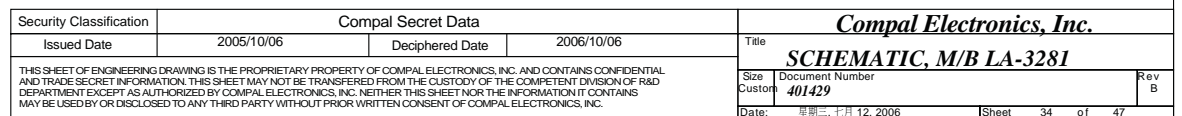
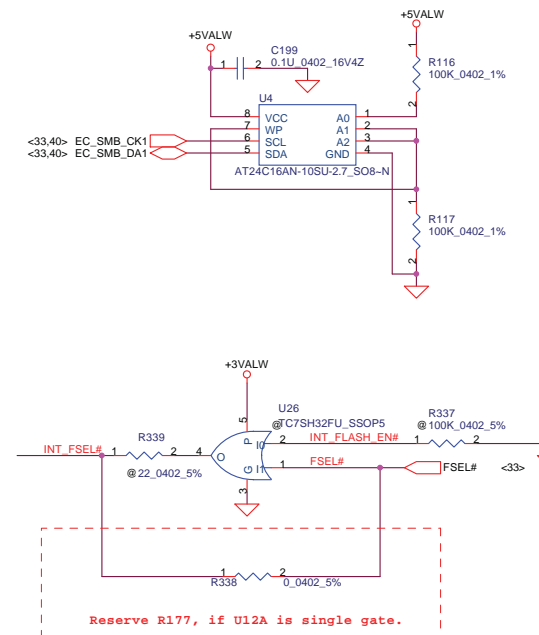
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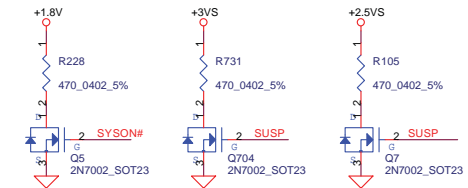
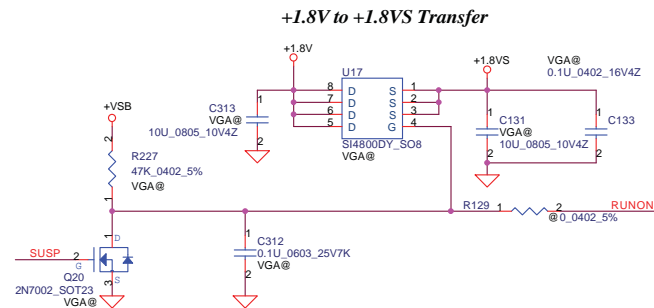
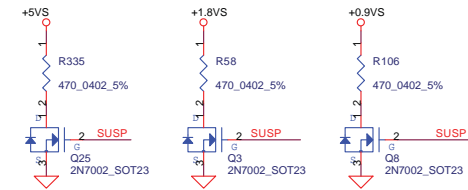
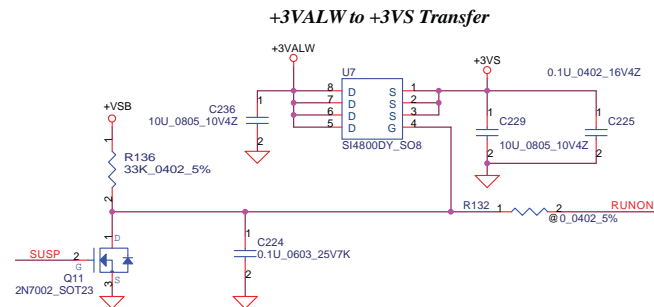
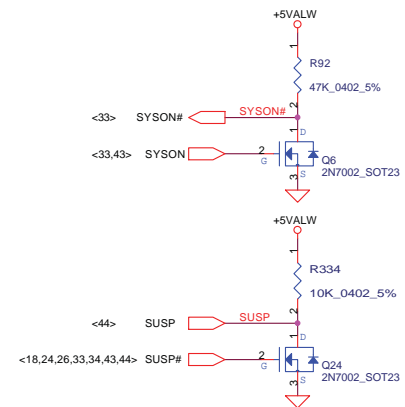
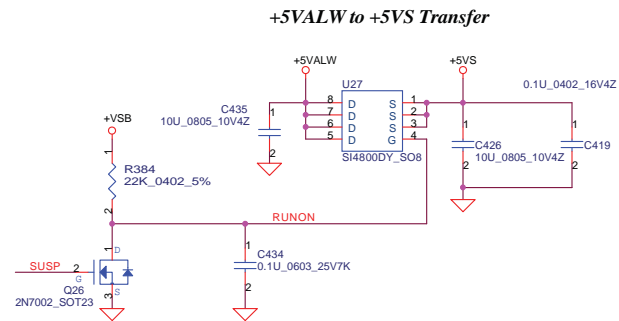
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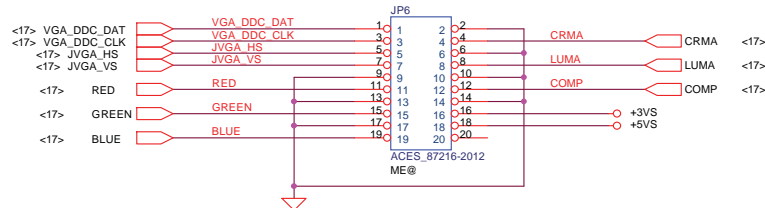




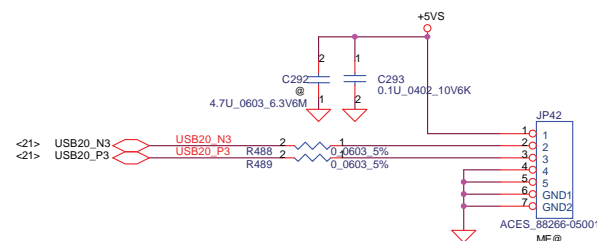


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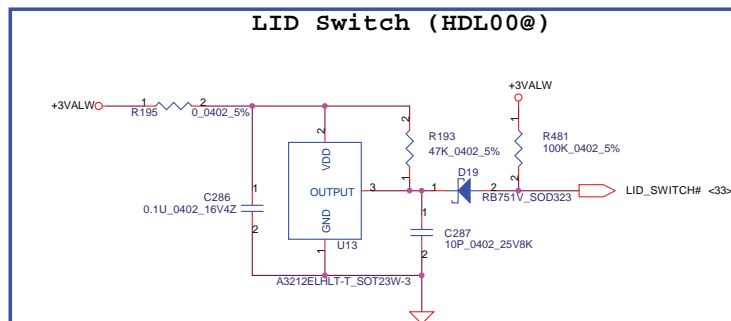
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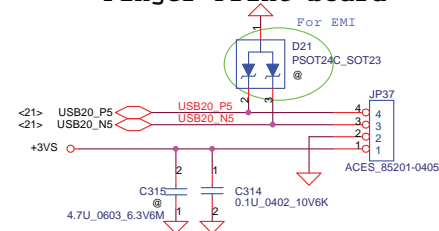
CMOS Camera Conn



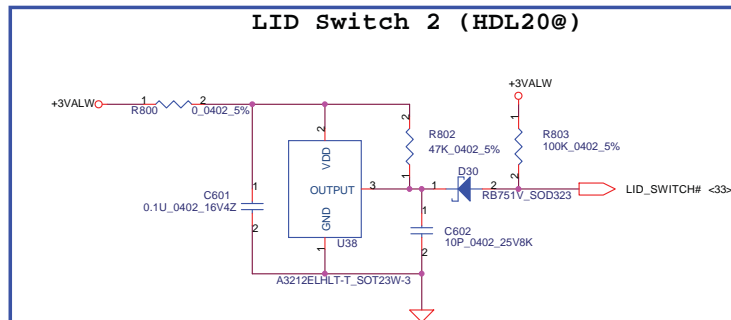
LID Switch (HDL00@)



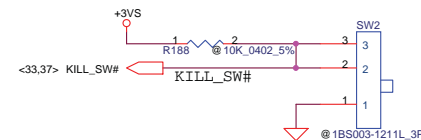
Finger Print board



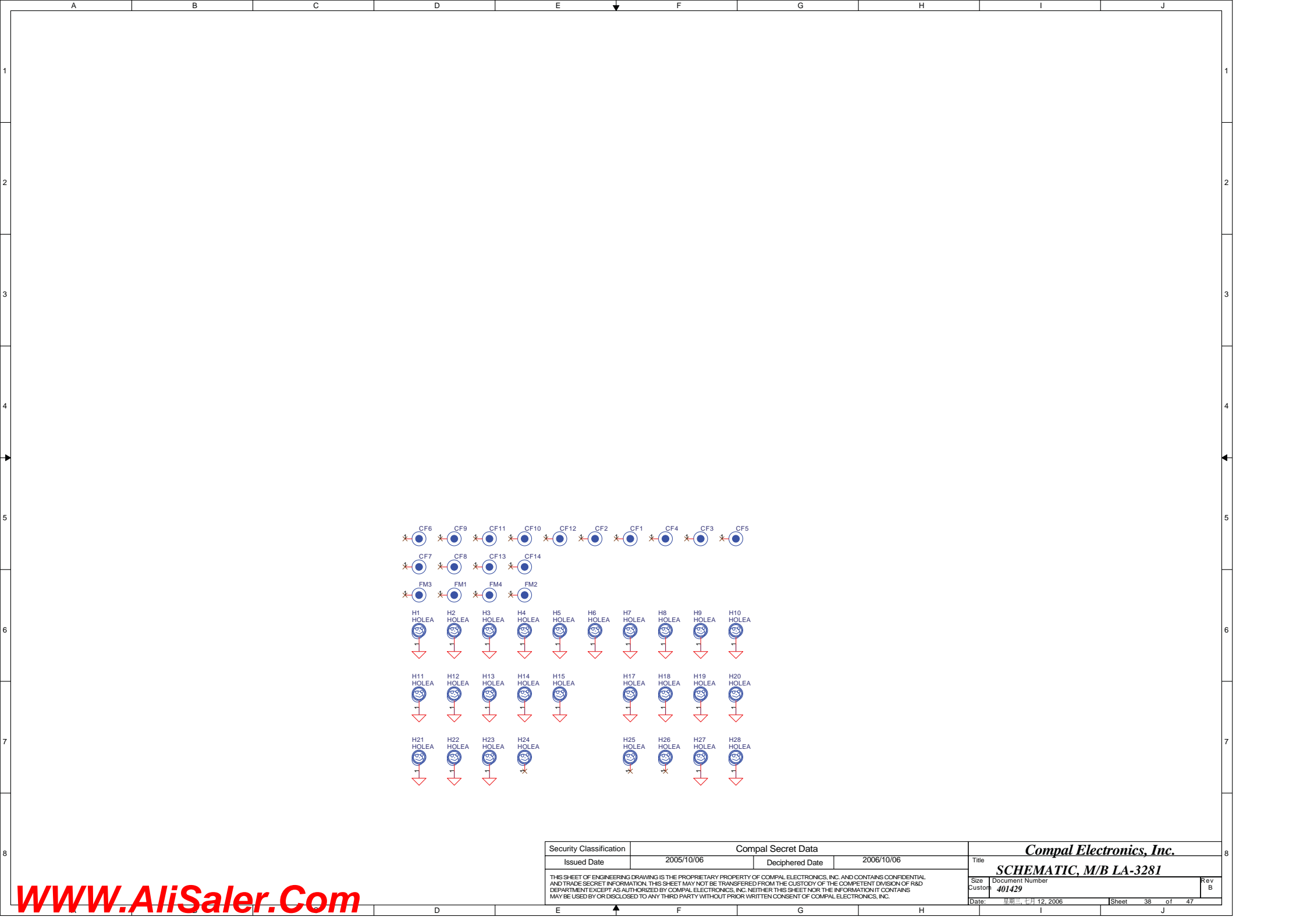
LID Switch 2 (HDL20@)



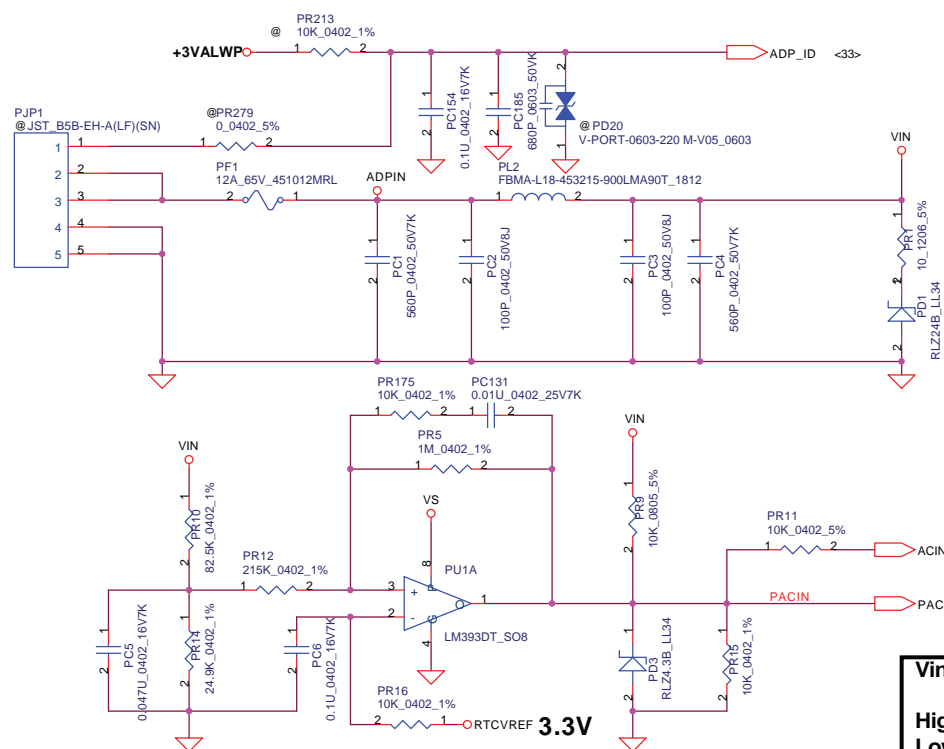
Kill Switch



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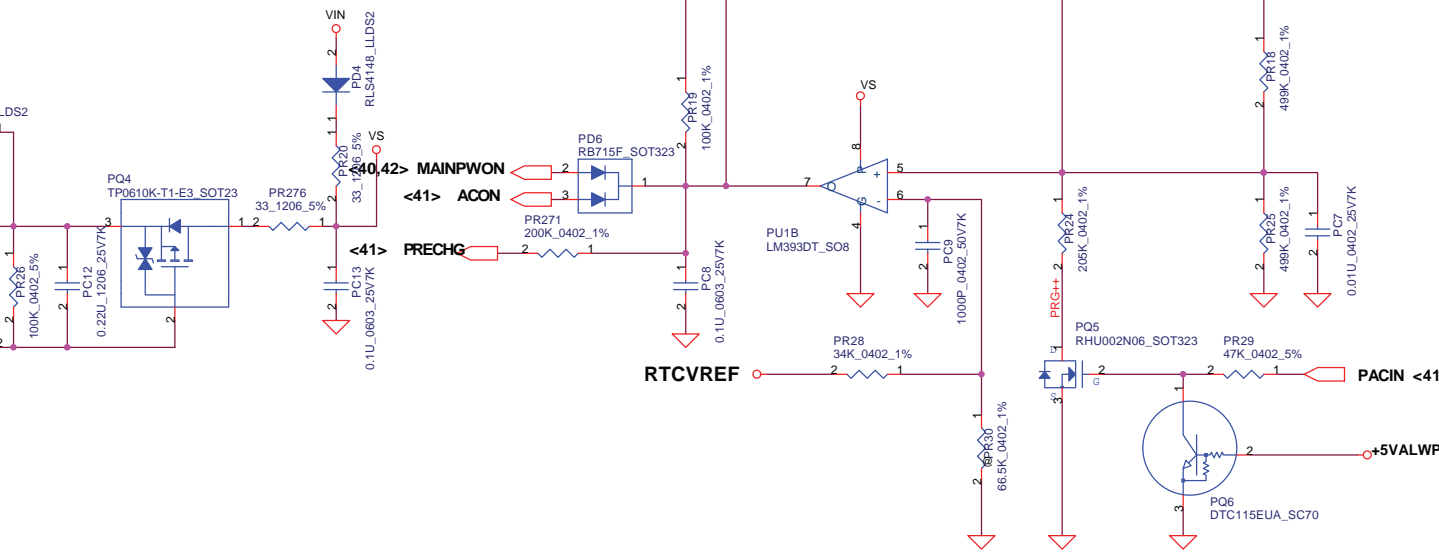
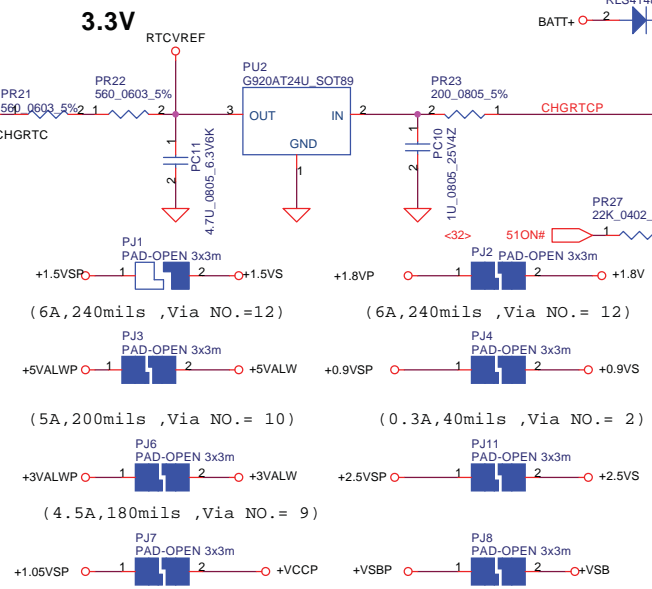
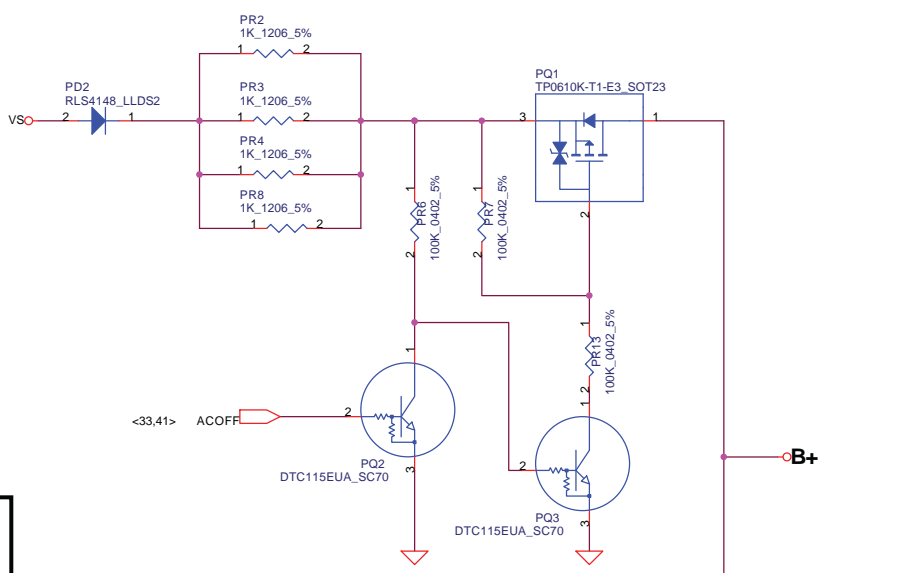


ACIN

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L->H	14.936V	15.381V	15.814V

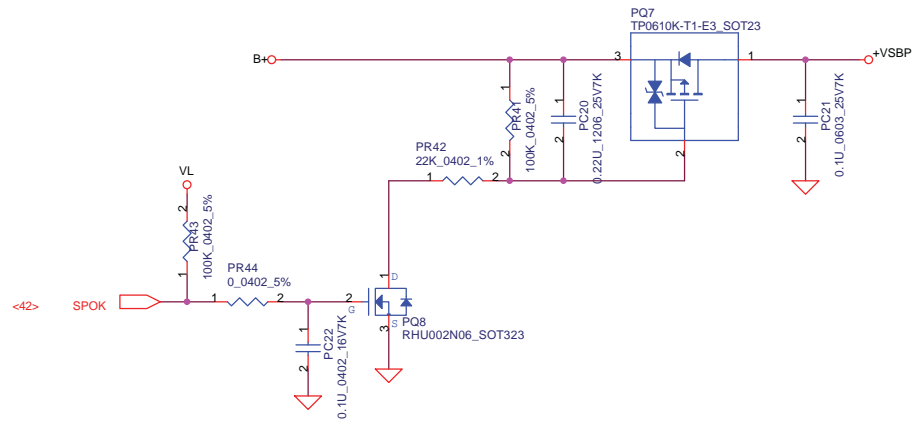
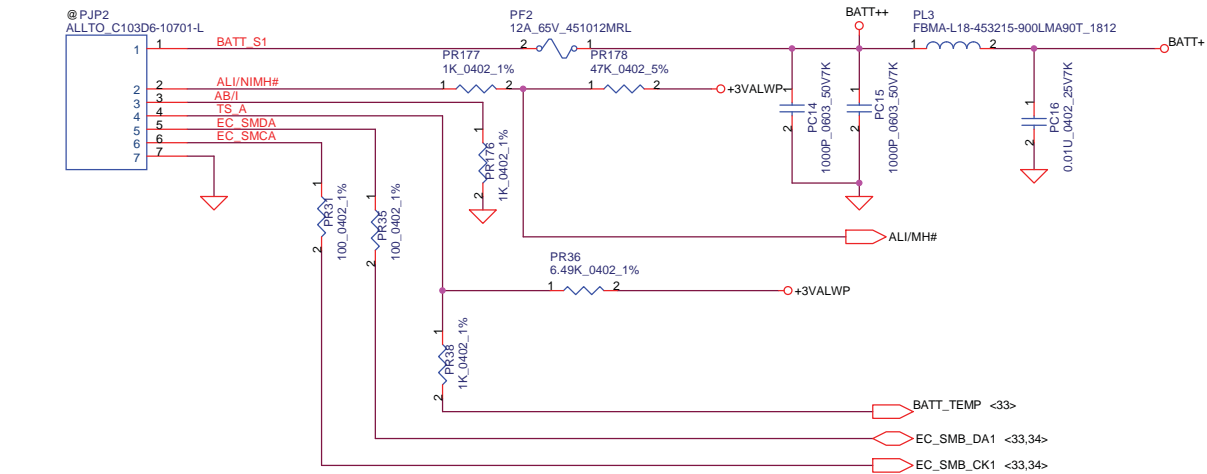
BATT ONLY

	Min.	typ.	Max.
H->L	6.138V	6.214V	6.359V
L->H	7.196V	7.349V	7.505V

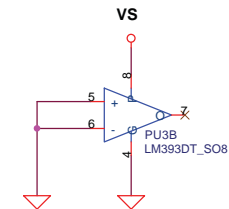
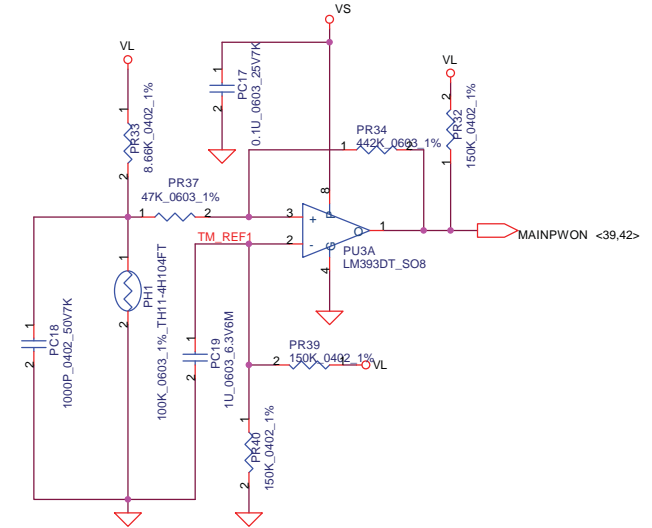


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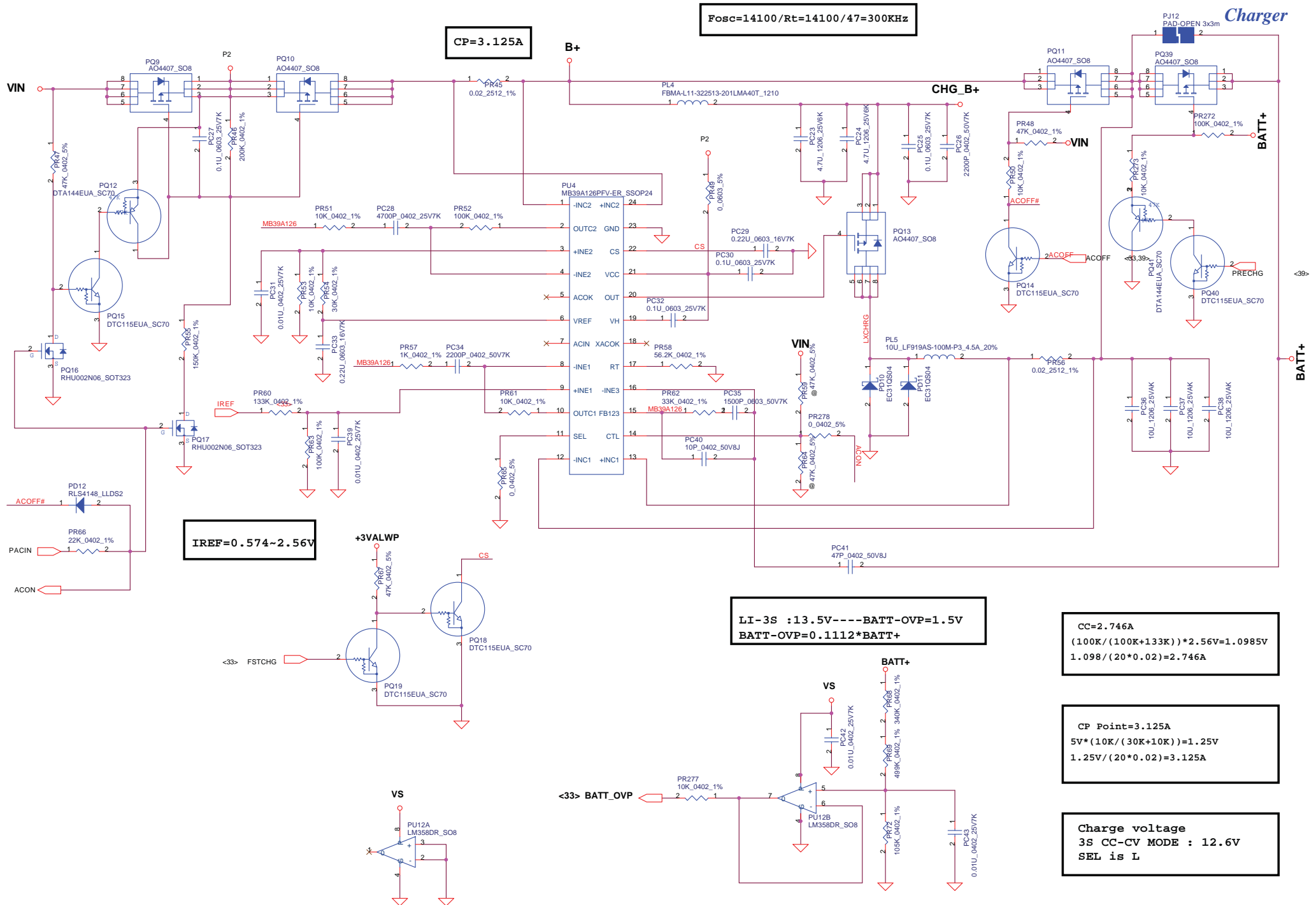
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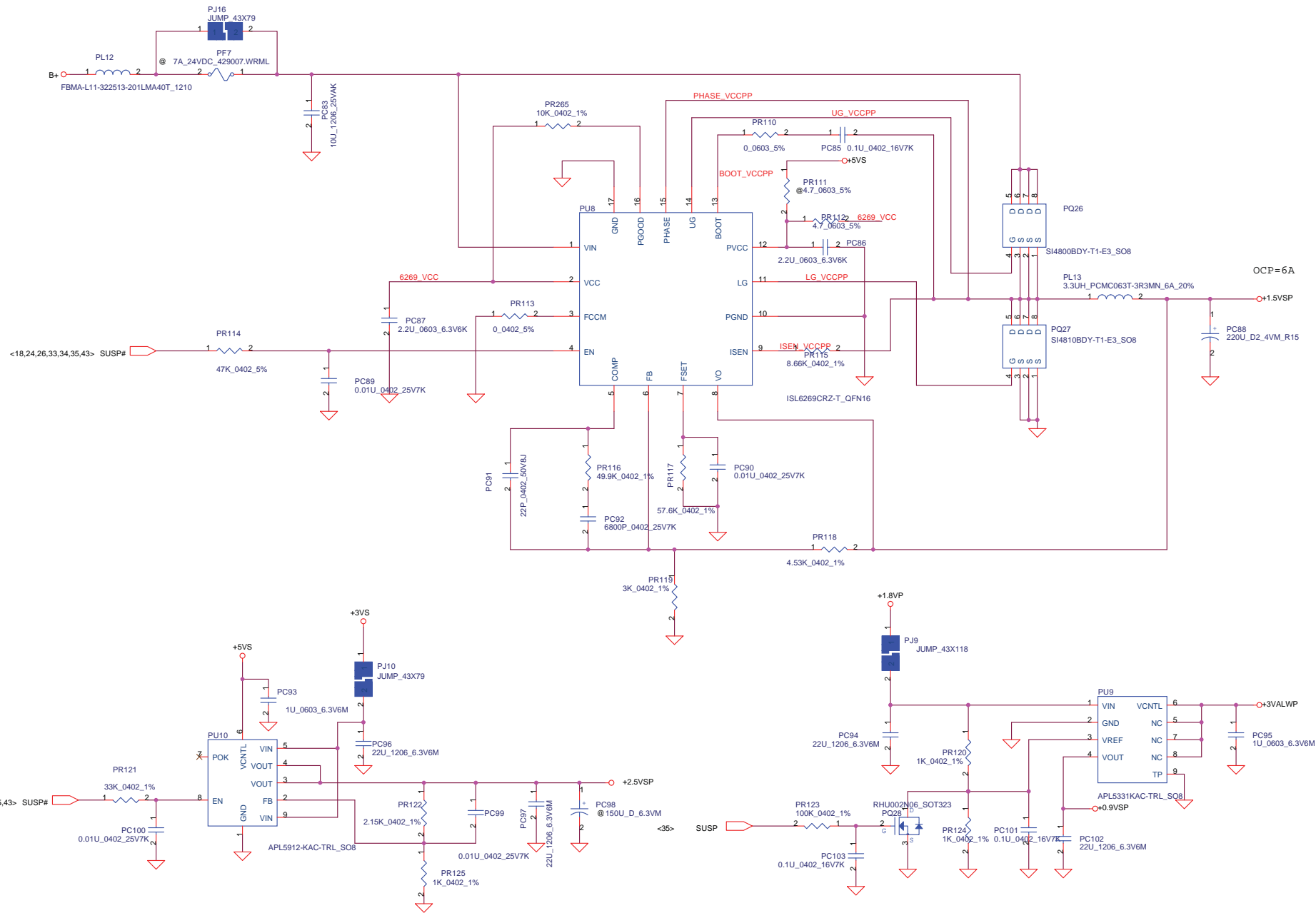
PH1 under CPU botten side :
CPU thermal protection at 85 degree C
Recovery at 70 degree C



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Version change list (P.I.R. List)

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Item	Fixed Issue/Reason for change	Rev.	PG#	Modify List	B.Ver#	Phase
A Test						
1	Copy schematic from HDL00					
2	Add 2nd BT connector	0.1	28	Add JP51,C60,Q706,Q705,Q708,R801,R810		
3	Add 2nd LID switch	0.1	36	Add U38,D30,R800,R802,R803,C601,C602		
4	Remove Front LEDs from MB	0.1	37	Del D6,D7,D8,D5,R190,R194,R191,R192,R189		
B Test						
5	Change audio solution from AD1986A to ALC861	0.2	29/30			
6	Add Front LEDs to MB(Reverse HDL00 Design)	0.2	37	Add D6,D7,D8,D5,R190,R194,R191,R192,R189		
C Test						
7	Sloving ICS pin 50, 51 no clock issue	0.3	15	Add R865 to U29.8 and grounded		
8	wake up on USB when AC-IN.	0.3	31, 33, 37	1. Add R866, R867 2. change EC pin 90 from KS017 to EC_GPIO4A 3. connect R866, R867 pin2 together, and net name is USB_ON#. 4. change syson# to USB_ON#, and control U9, U10 and U25.		
9	EMI solution	0.3	16	1. change L14 from 0 ohm to bead 300 ohm 2. change C295 from 0.8pF to 470pF		
10						
11						
12						
13						
14						

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